how big can you dream?™

cadence

On-chip RF Isolation Techniques

Tallis Blalack, Youri Leclercq, Patrick Yue[1]

[1]Atheros Communications, Inc.

BCTM 12.1 **October 1, 2002**

Key Take-away Point

cadence

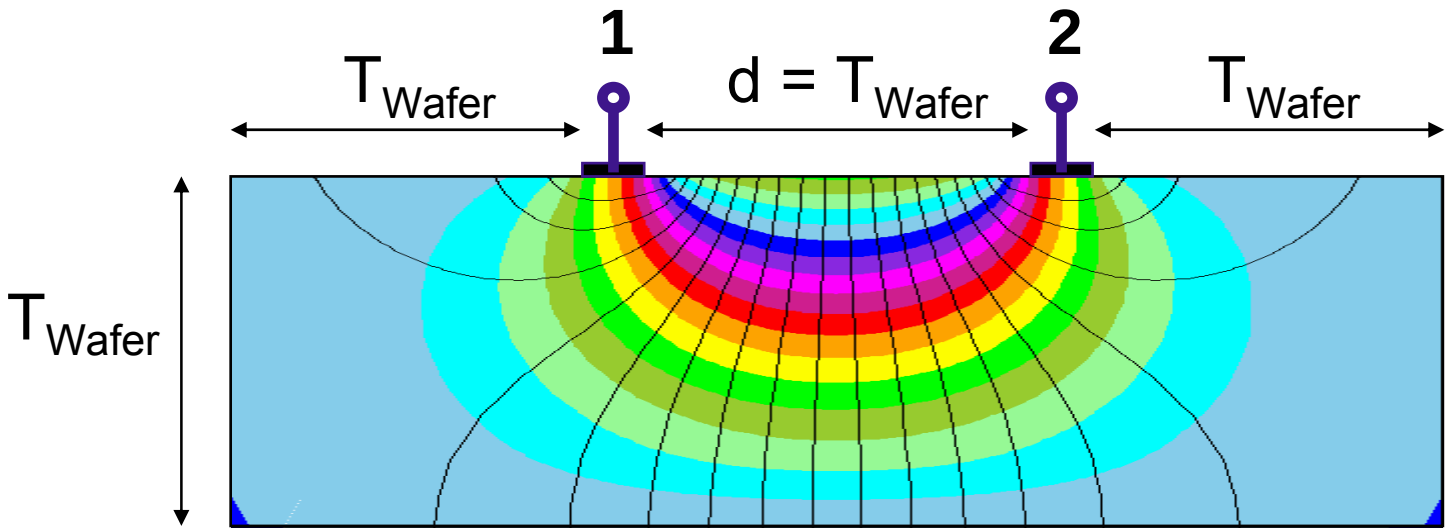
IT DEPENDS!

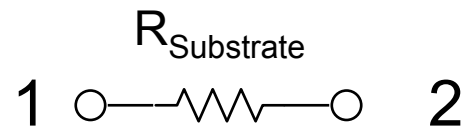
- What is the maximum isolation I can achieve?
- How do I win the isolation argument with my co-workers?
- Will I get anything useful out of this talk?

Outline

- Technology impacts
  - Technology overview
  - Buried layers
  - Triple wells
- Grounding effects
- Guard rings
- Shielding
  - Patterned ground shield
- On-chip decoupling capacitance
- Summary

Lightly-Doped Wafer Resistivity





Non-conductive Backside

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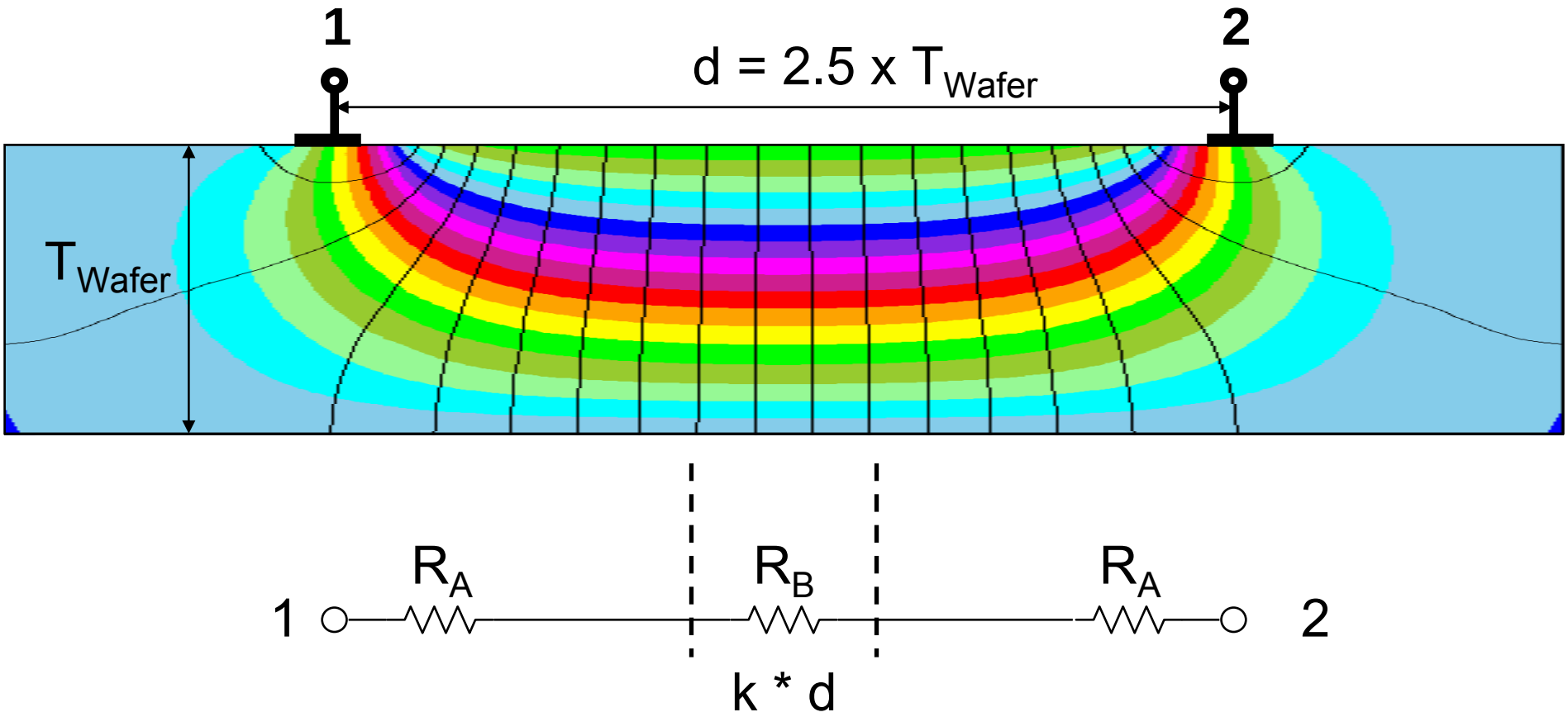
Lightly-Doped Wafer Resistivity



Non-conductive Backside

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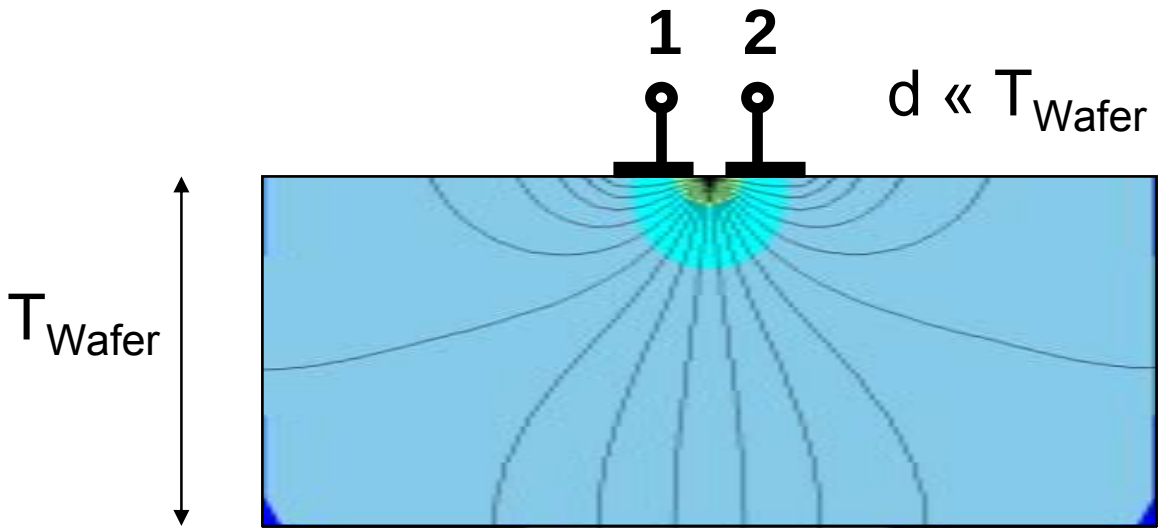

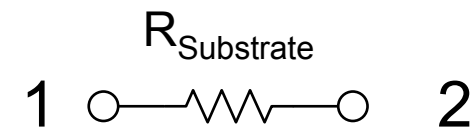

$d_2 = 2 * d_1$: $R_2 < 2 * R_1$

Non-conductive Backside

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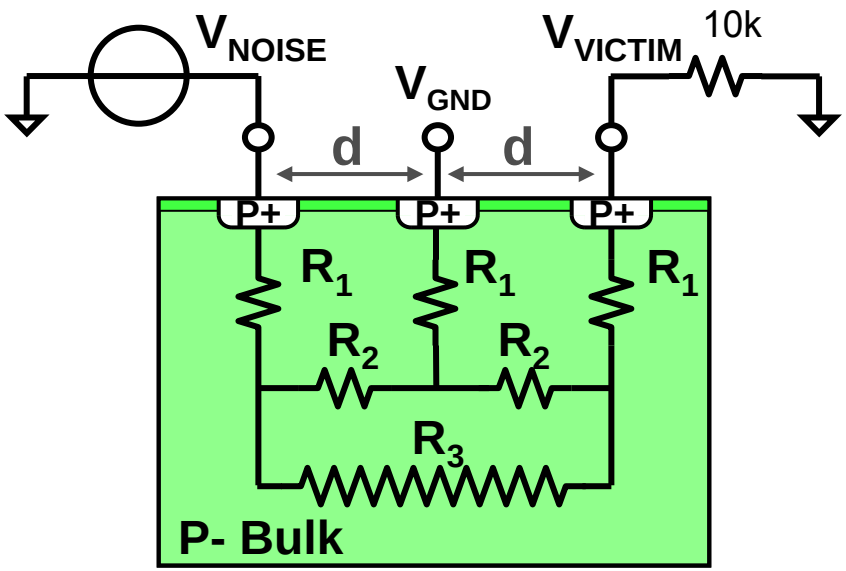
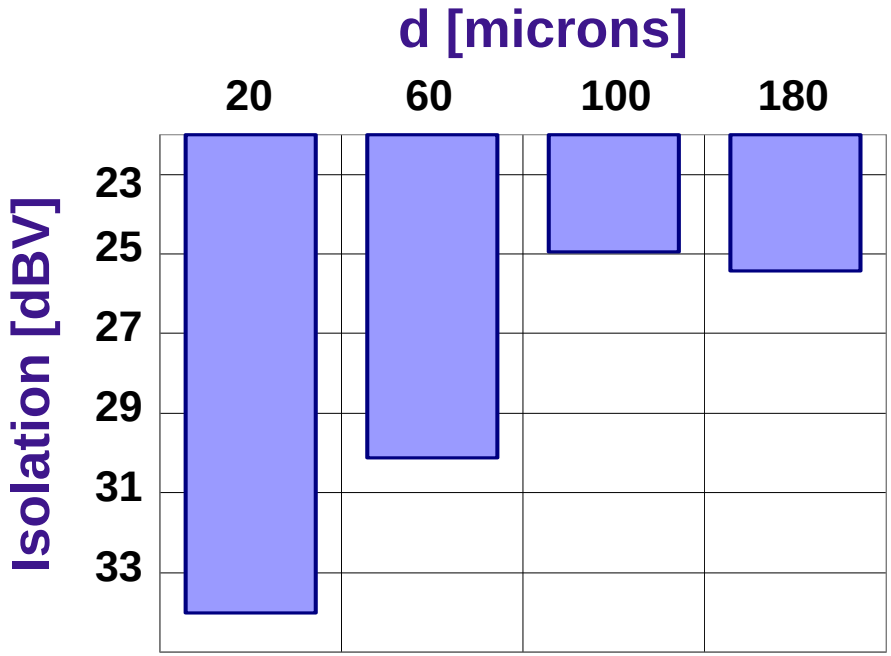
Lightly-Doped Substrate Isolation





- Lightly doped material
- Maximum isolation when source and victim are closer to the guard band
- Bonding inductance will affect isolation

$$Isolation = 20\log\frac{V_{victim}}{V_{noise}}[dBV]$$

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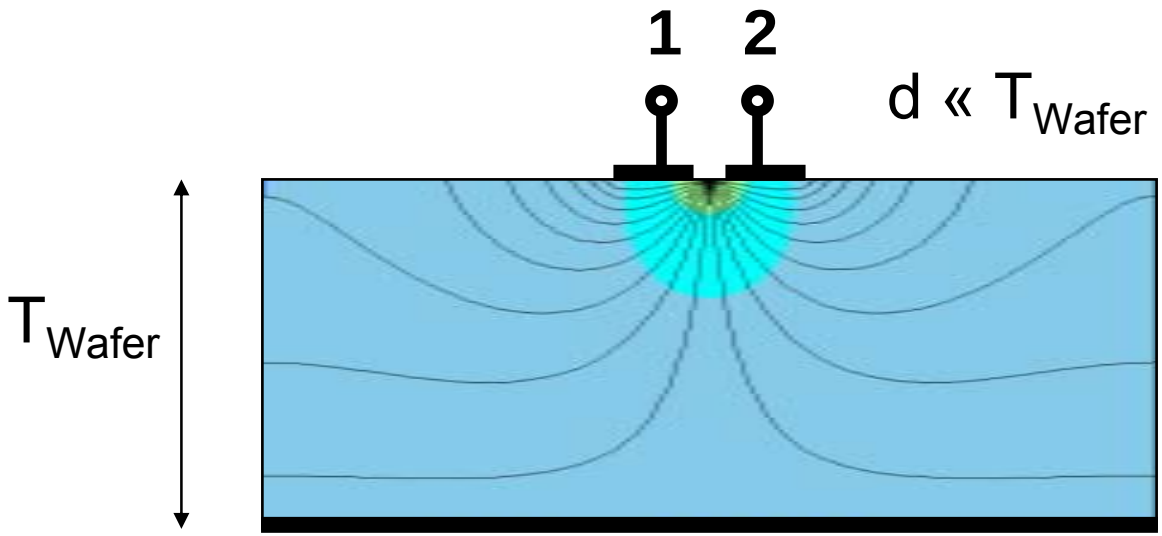
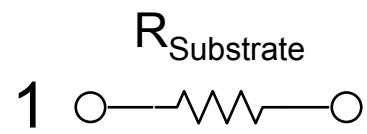
Lightly-Doped Wafer Resistivity

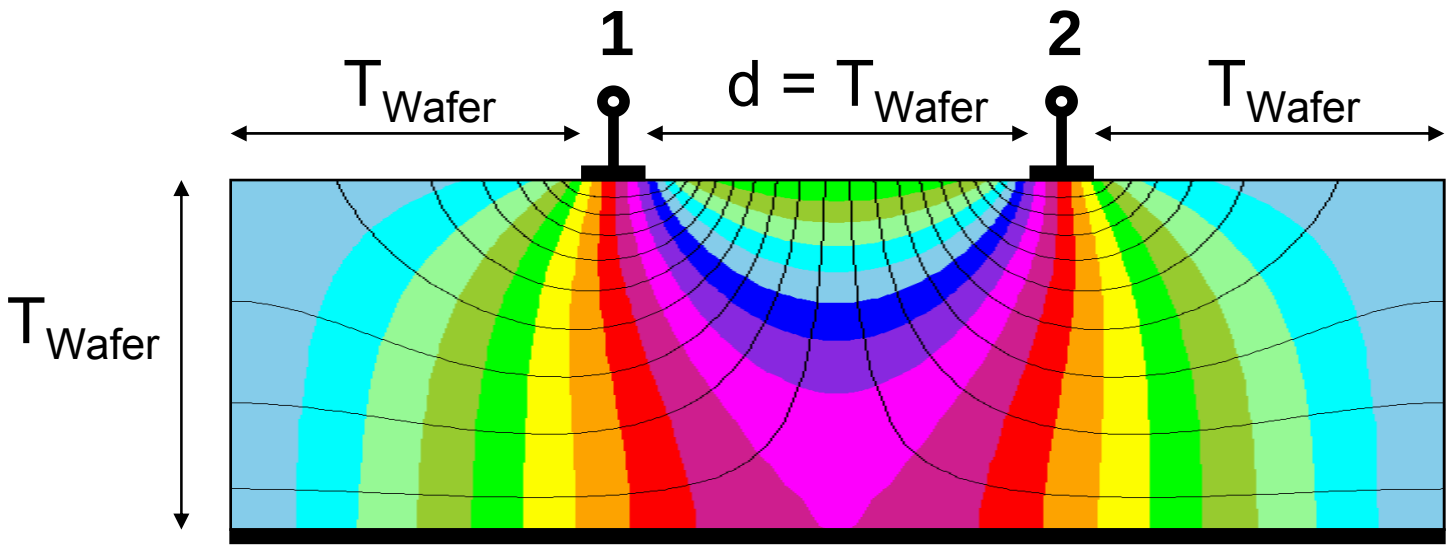




$$d_2 = 2 * d_1 \quad : \quad R_2 < 2 * R_1$$

Floating Conductive Backside

Lightly-Doped Wafer Resistivity



Floating Conductive Backside

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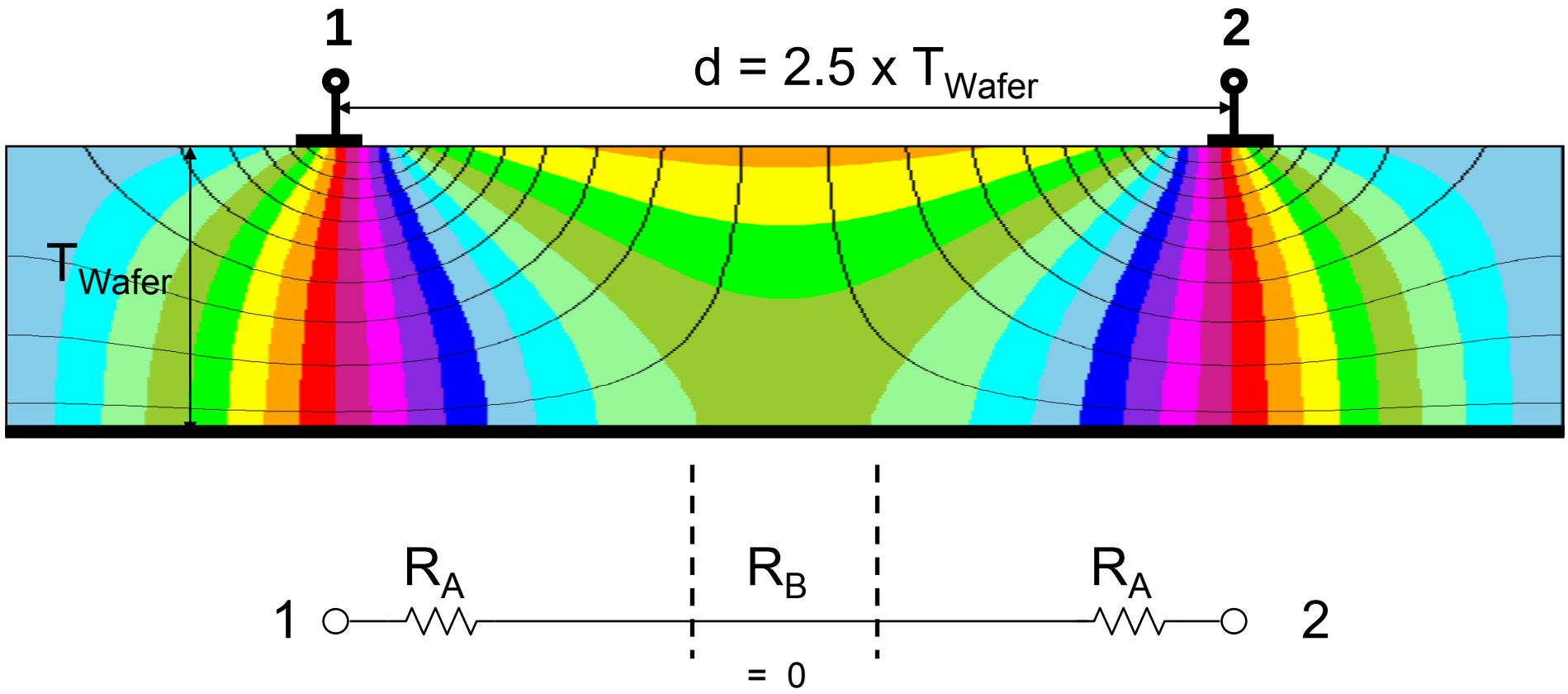
Lightly-Doped Wafer Resistivity



Floating Conductive Backside

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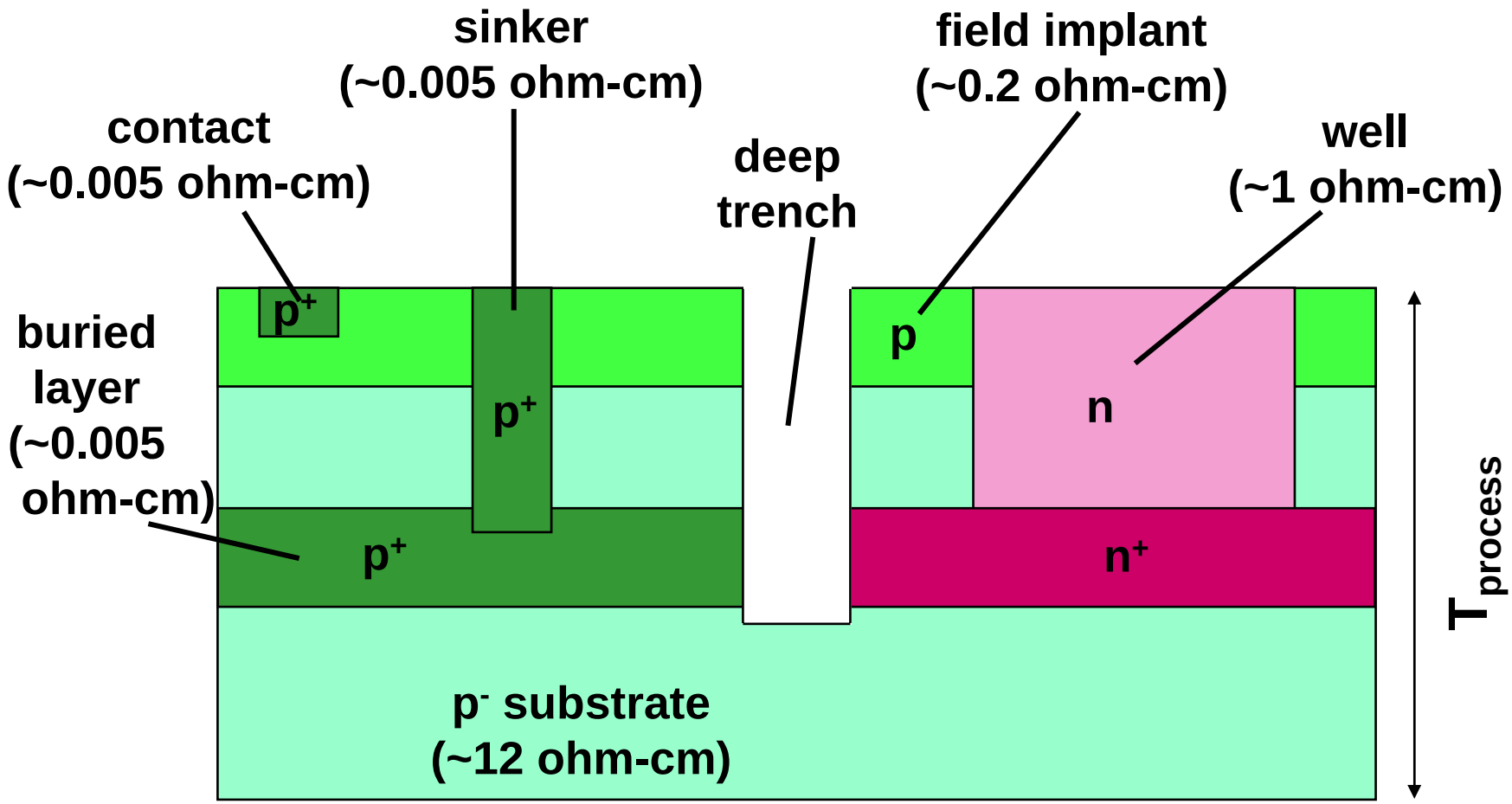
BiCMOS Technology Basics



F. Clement in J. Huijsing et al, KAP, '99

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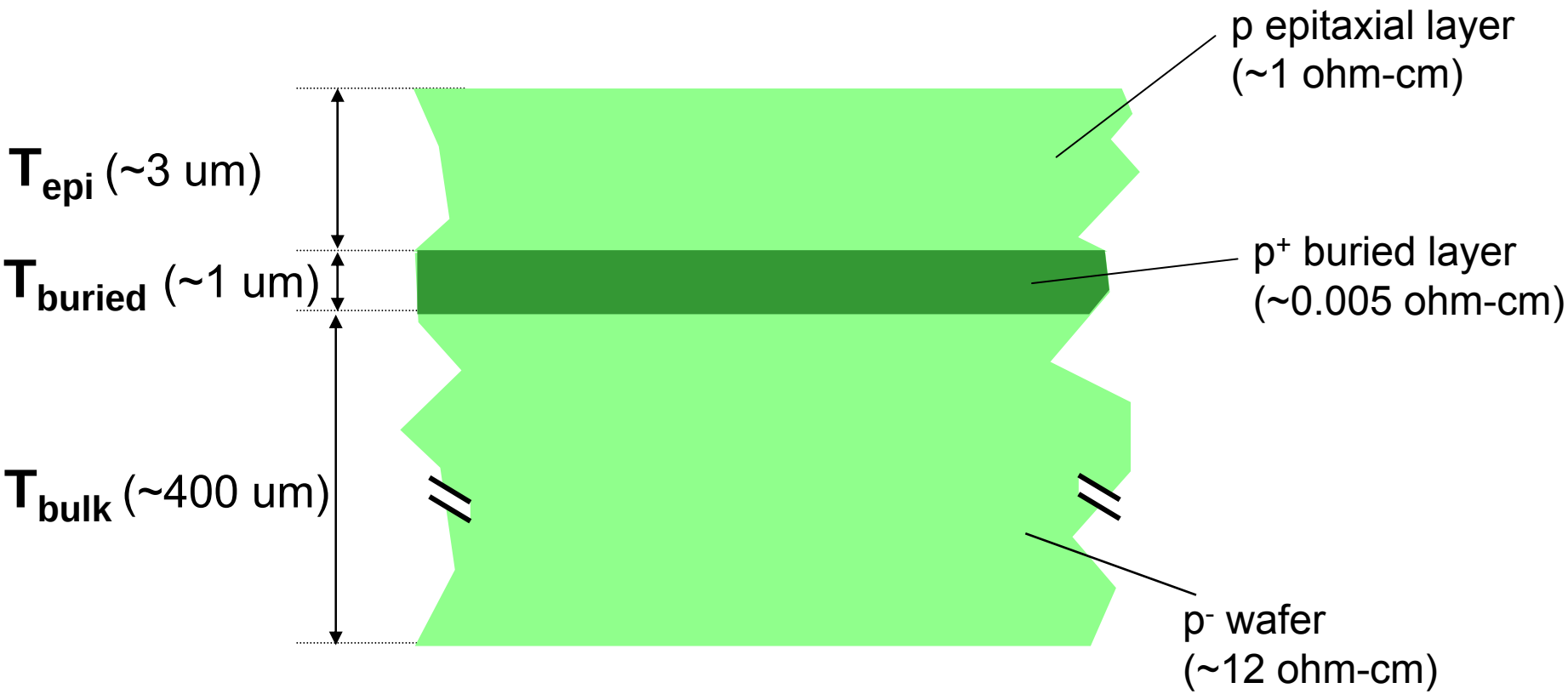
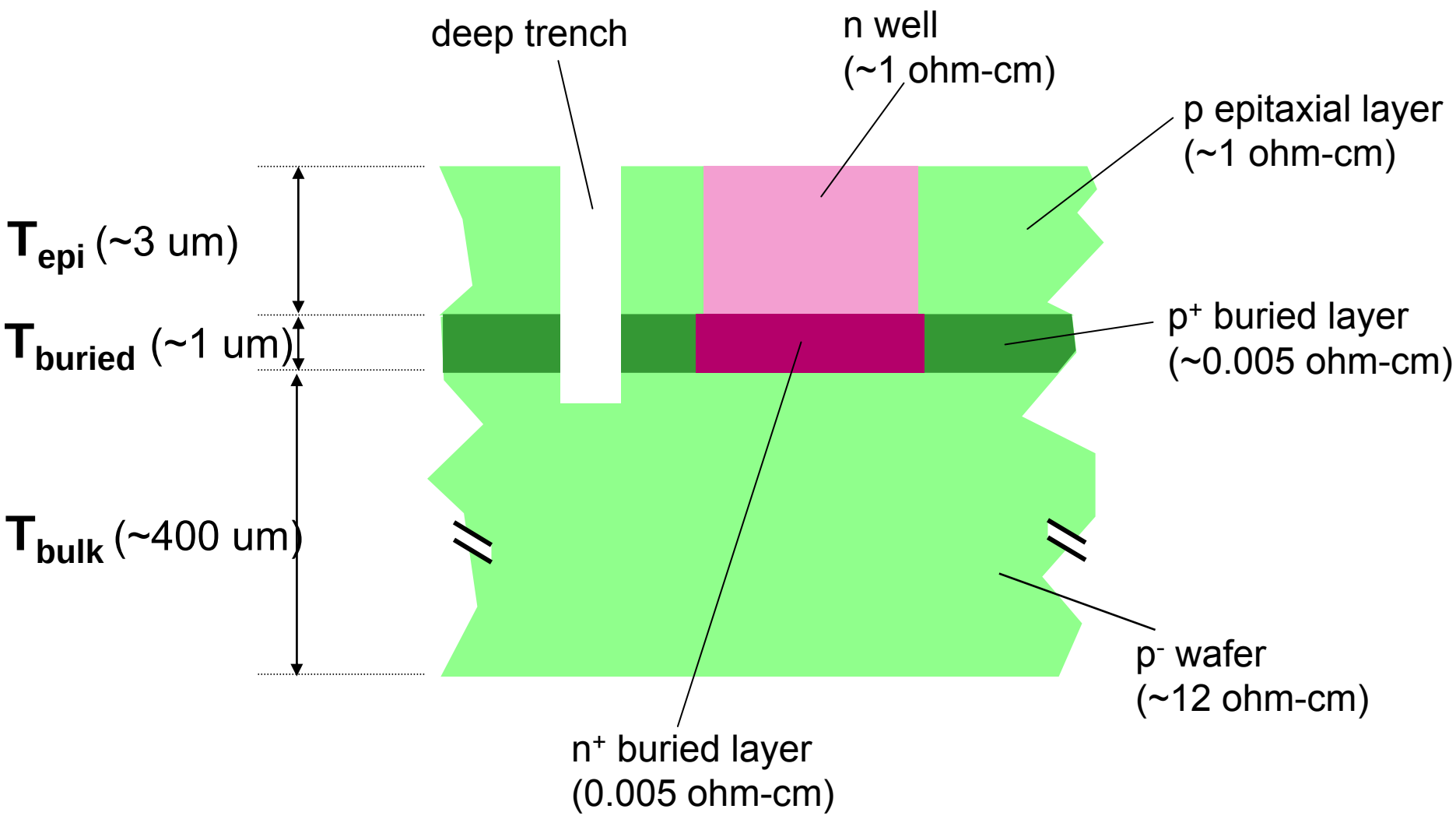
Buried Layer with Lightly-Doped Wafers



$$R_{bulkepi} \sim 5 \times R_{buried}$$

Breaking the Buried Layer



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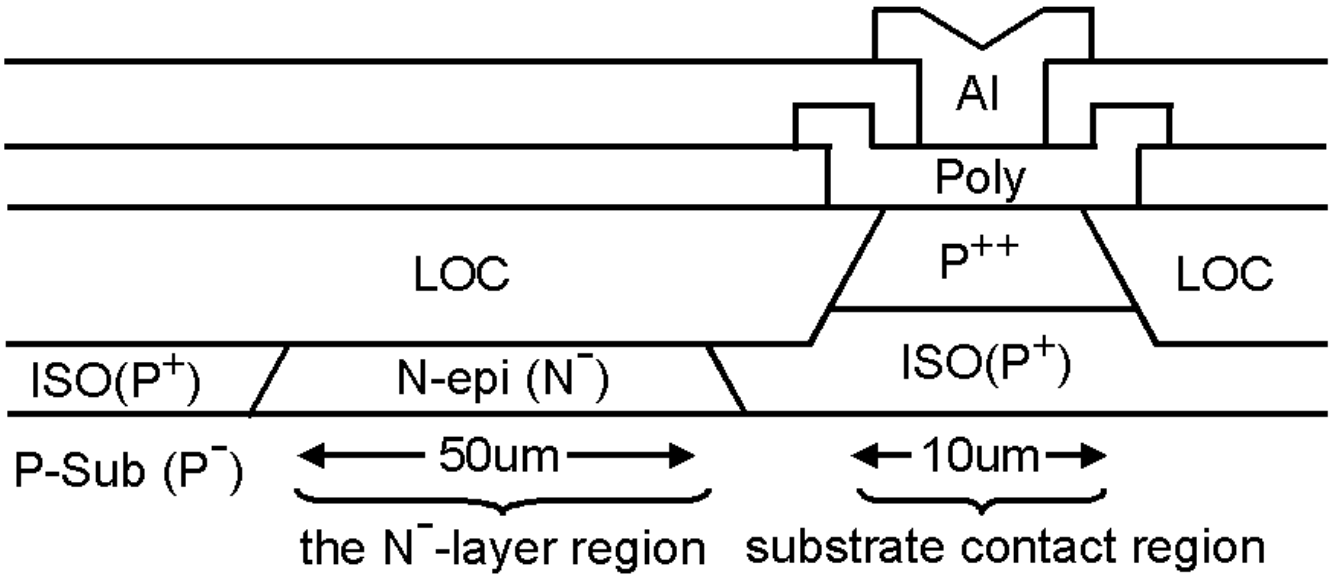
Sony: 622 Mb/s Optical Receiver IC

Isolation for High Sensitivity

A trans-impedance amplifier is isolated
from the other circuit blocks

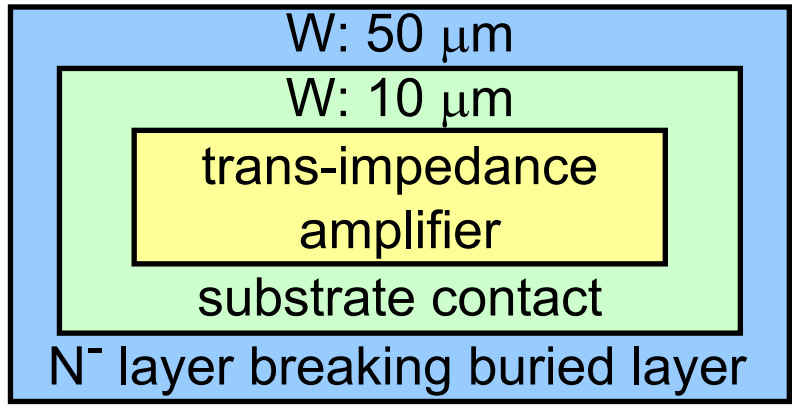
(1) **substrate contact region**
(2) **the N^--layer (removed P^+) region**

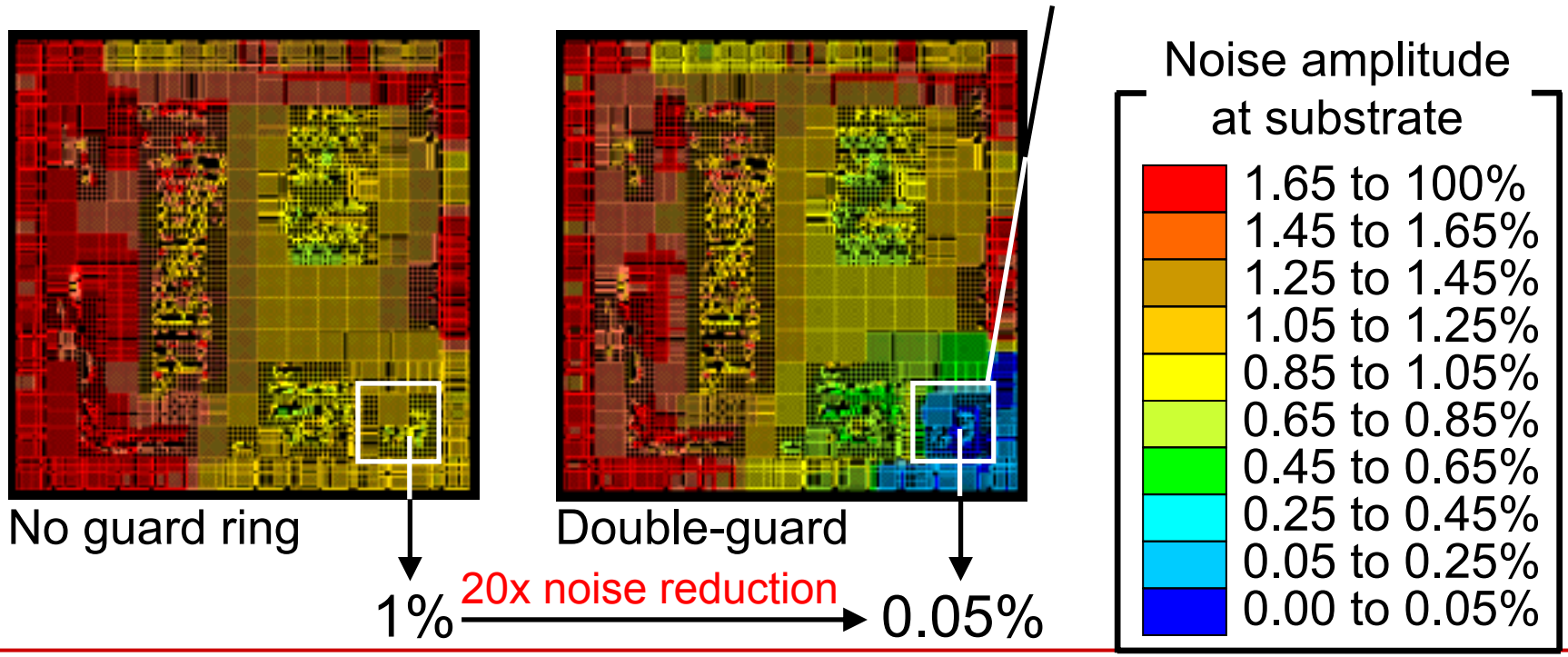


T. Takeshita, ISSCC 2002 Tallis Blalack, BCTM 2002, Paper 12.1

Sony Noise Simulation

- Substrate noise distribution
  - SubstrateStorm
- Noise source injection points
  - Logic ground
- Noise source amplitude of 100%





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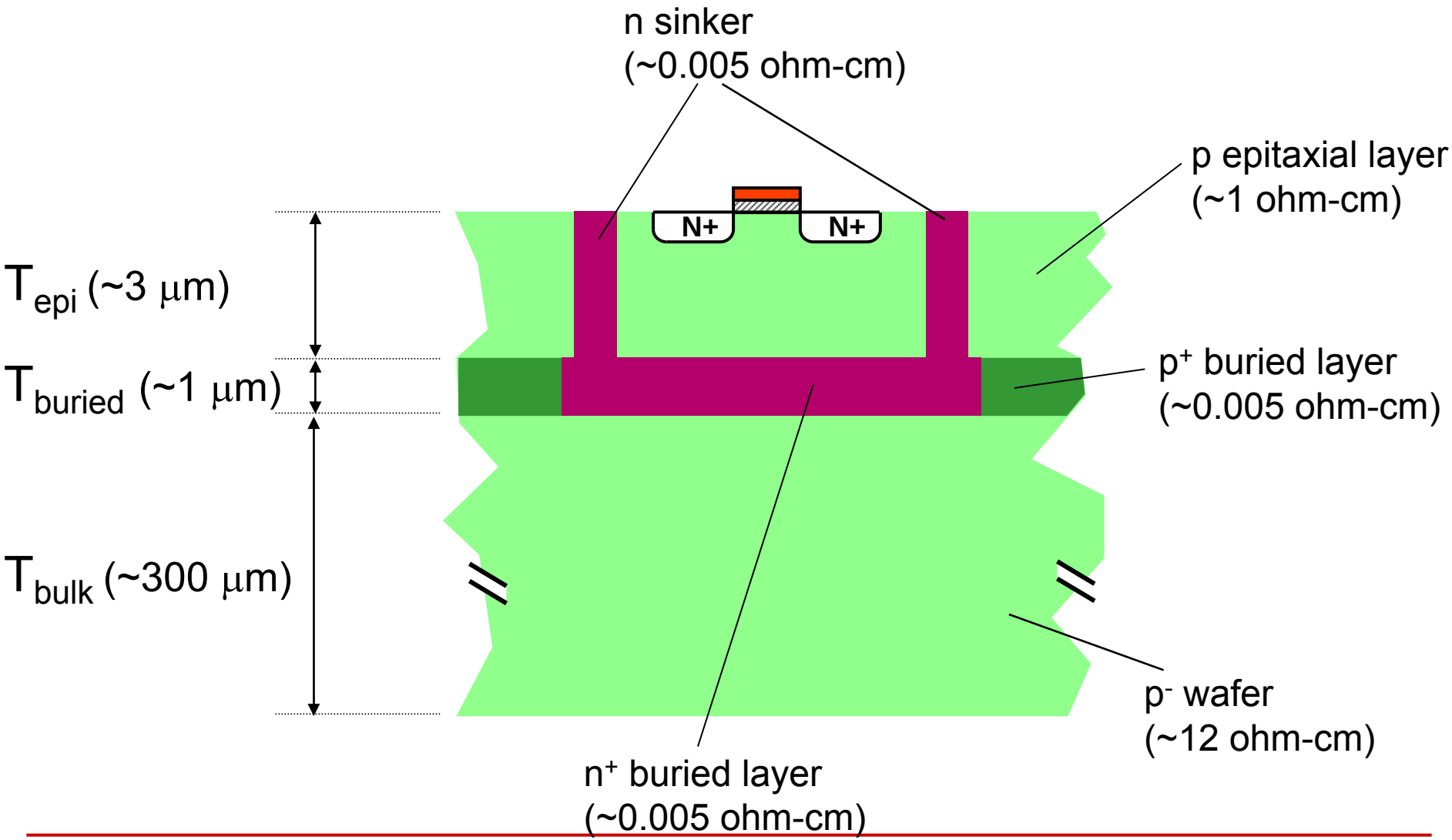
NMOS: Triple Well Isolation



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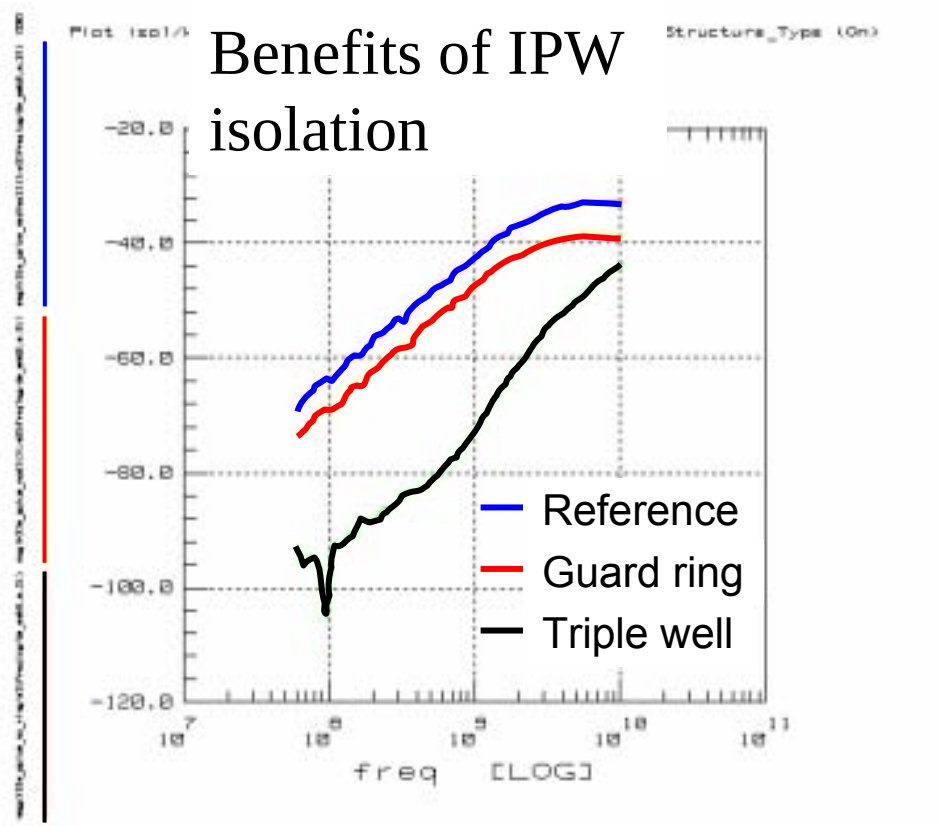
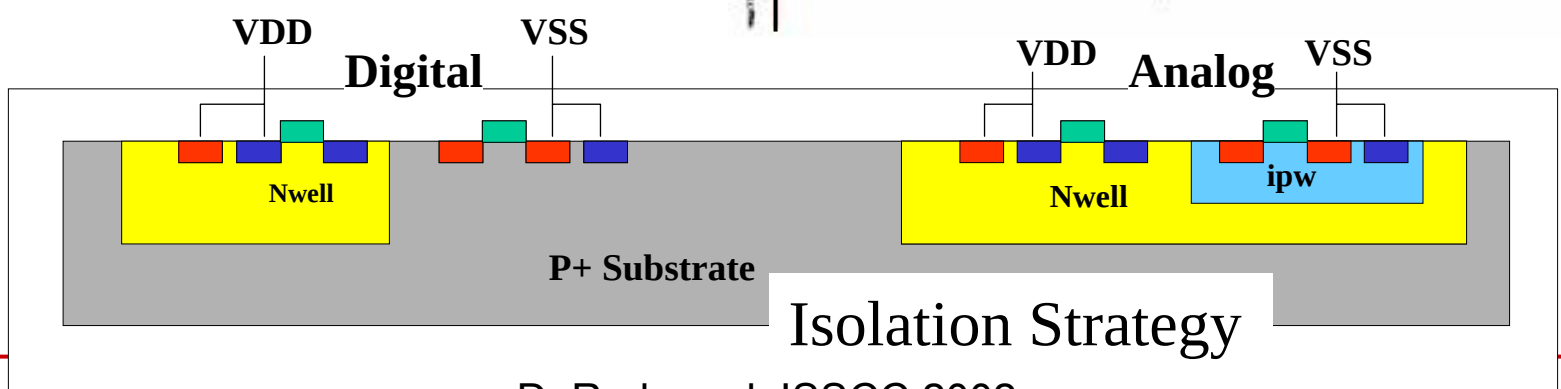
Motorola: GSM/GPRS Baseband IC

Process technology **HiP7LP** :
(compatible with TSMC)

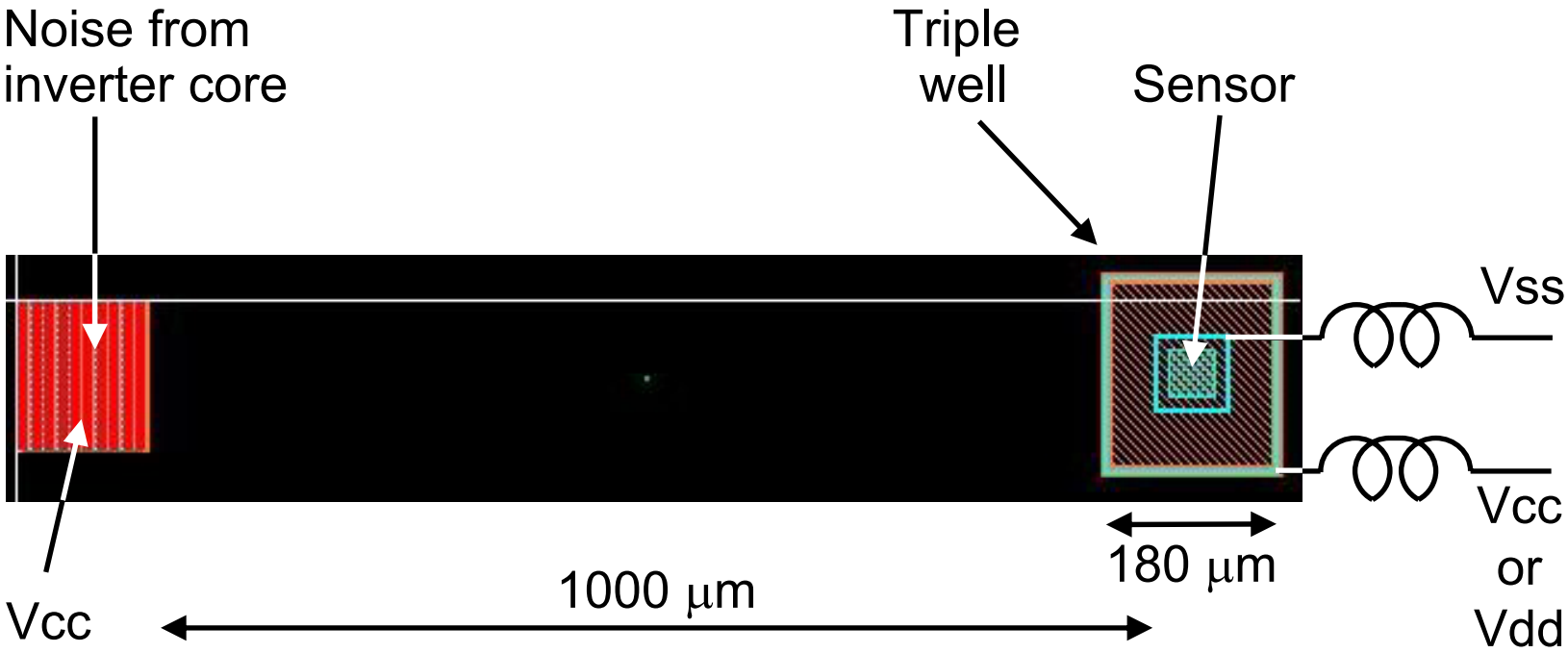
Gate length *Lpoly*	0.13 μm
Single gate Ox	30 A
Dual gate Ox	50 A
Supply voltage	1.6 to 3.0 V
Metal	5 layer Cu
Substrate	P+
Nwell resistors	700 ohm/sq
Salicided Poly res.	7.0 ohm/sq
Metal Cap	0.8 fF/μm^2





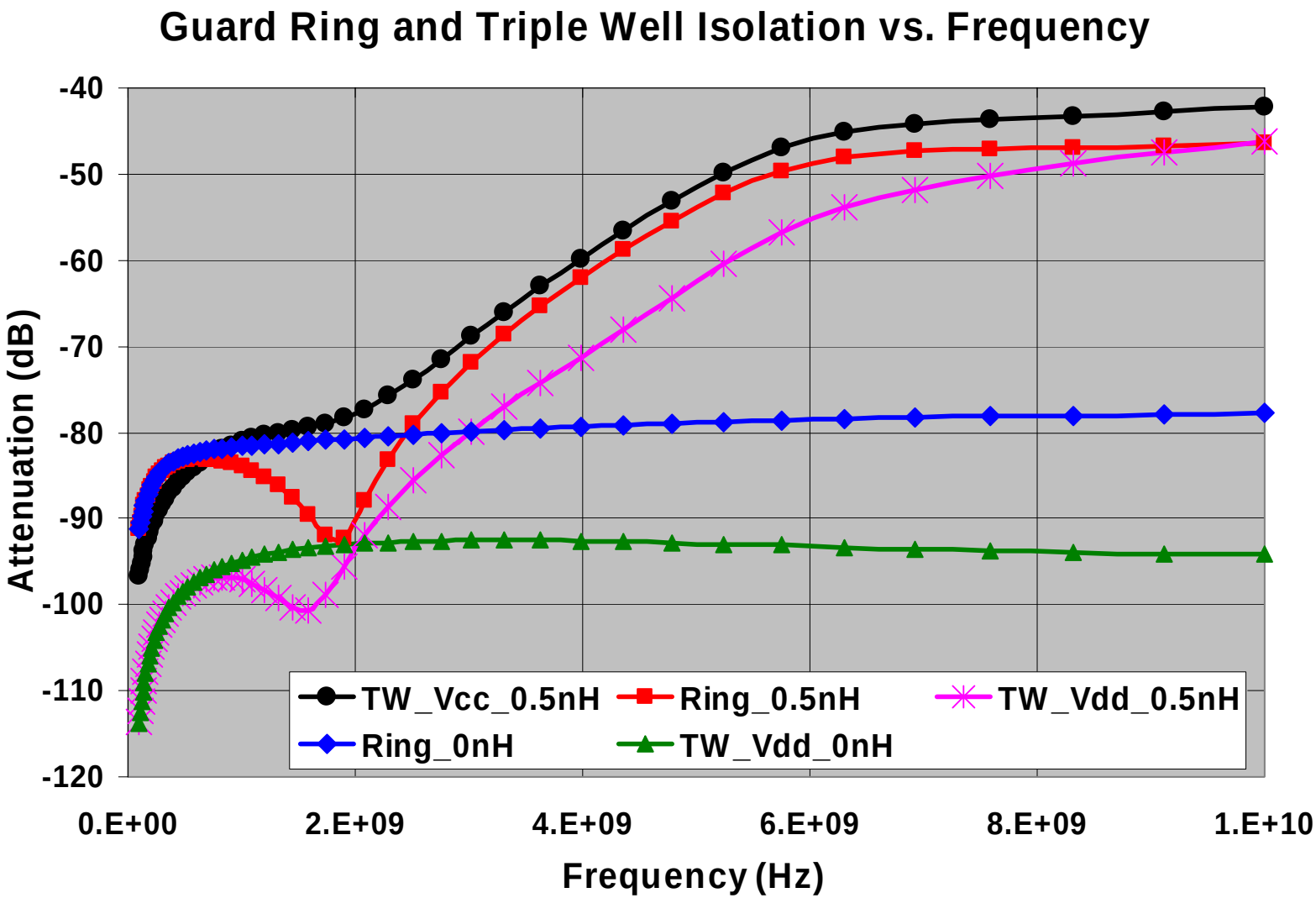
D. Redmond, ISSCC 2002 Tallis Blalack, BCTM 2002, Paper 12.1

Triple-well Simulation Structure



- Separate ground used for the digital core
- All simulations use SubstrateStorm with a 0.35 μm BiCMOS technology
- Remove triple well and compare with identical p+ guard ring

Package Effects on Triple-well Isolation



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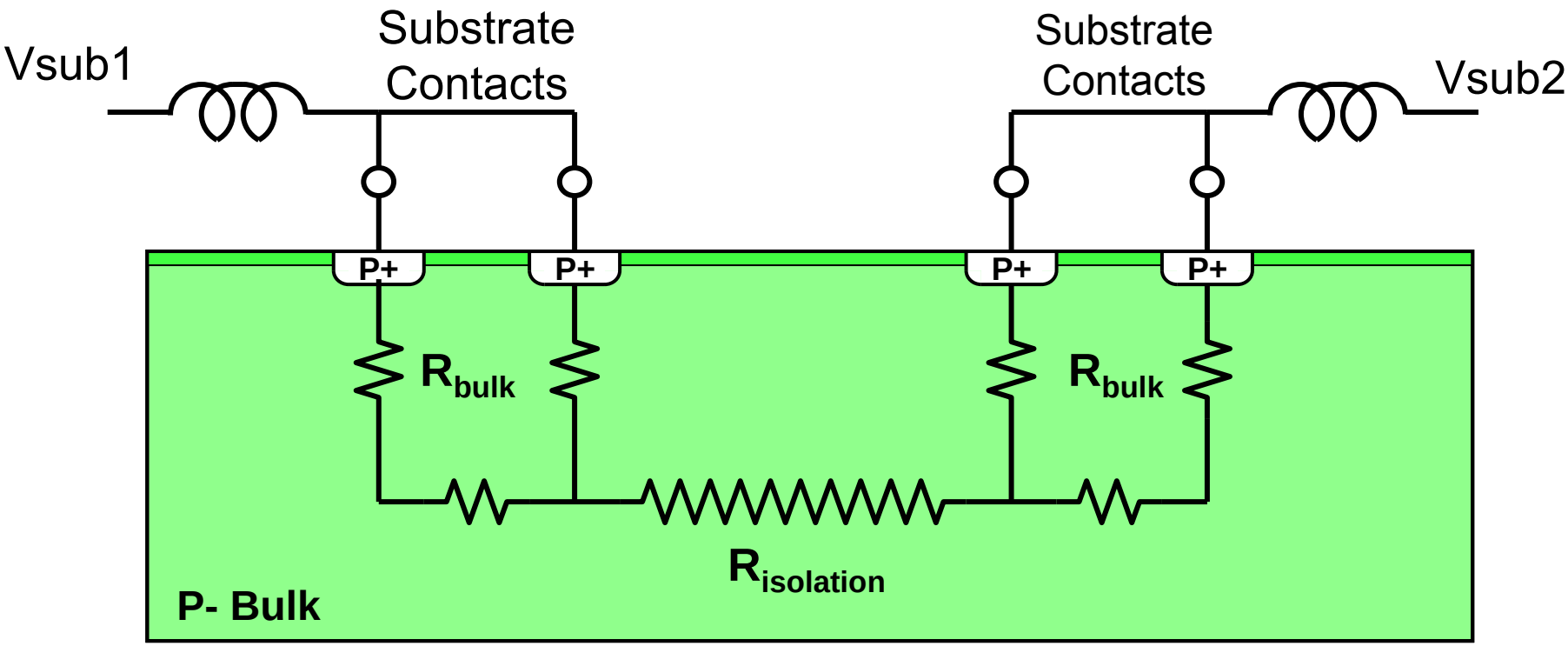
Grounding Effects



- Use multiple supplies to isolate areas
- Minimize inductance

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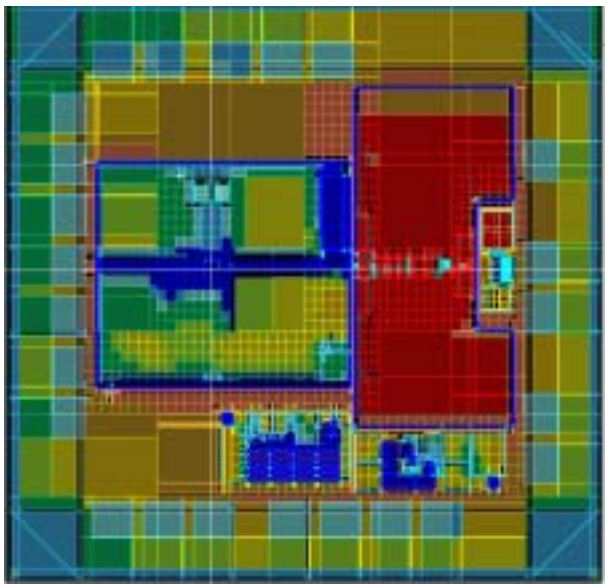
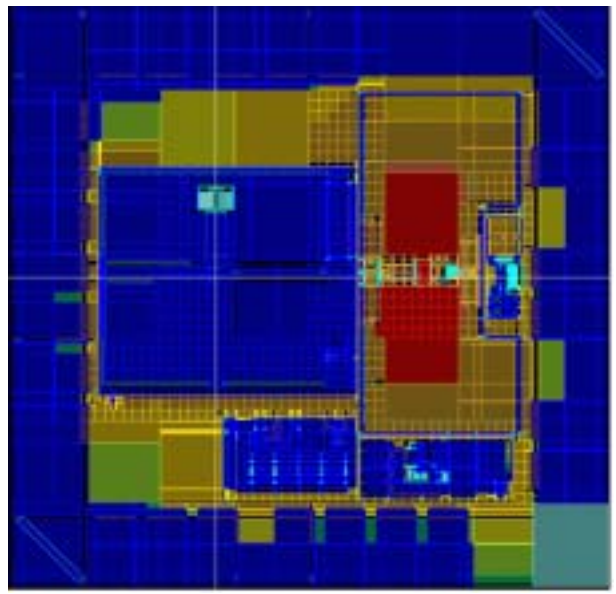
STMicroelectronics: LNA + Mixer Integration

- Initial design had one substrate ground
- Simulations showed too much noise coupling
- Separated supply regions to isolate LNA from mixer



One substrate ground



Two substrate grounds

A. Cathelin, DATE 2002

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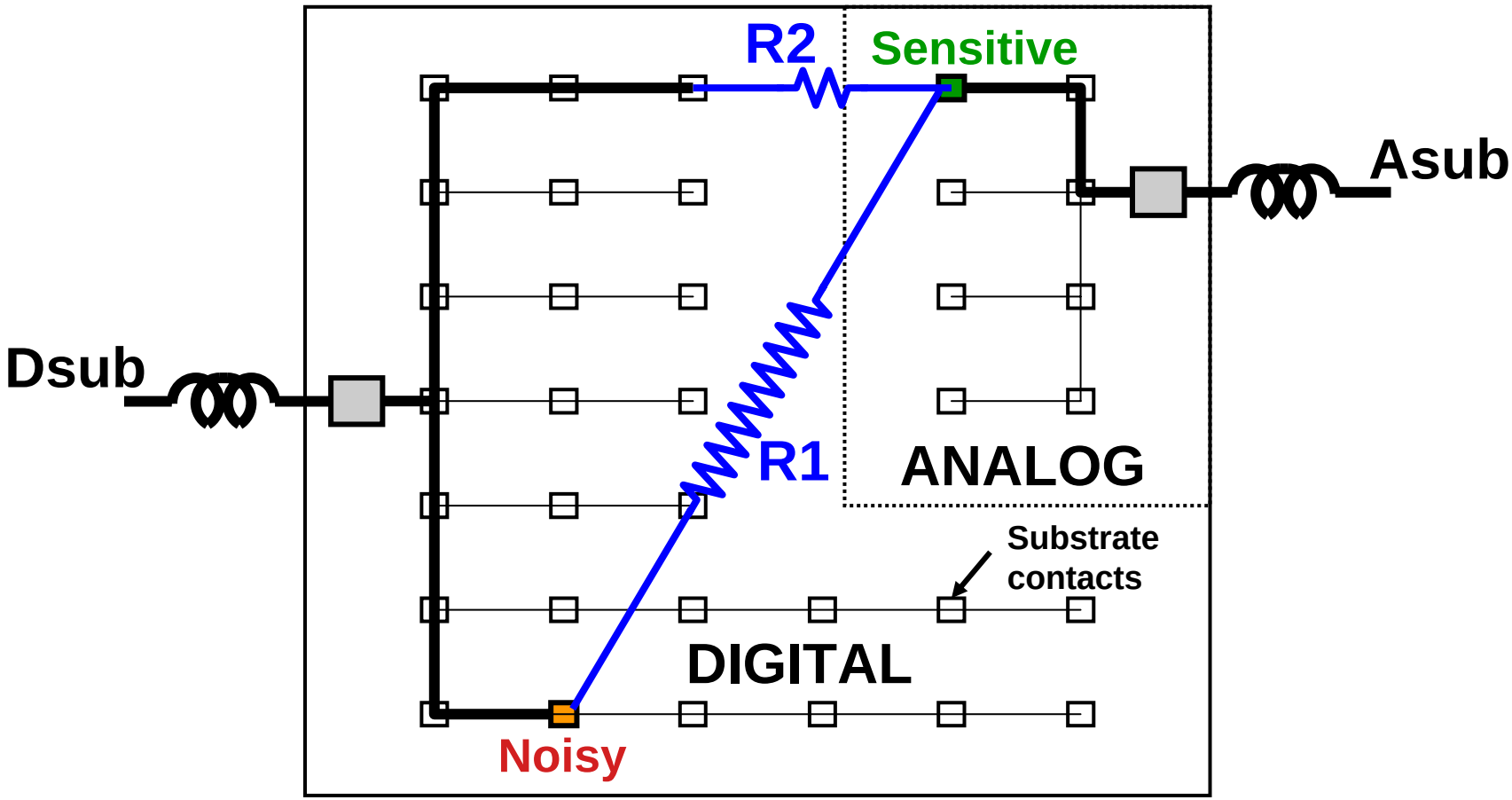
Coupling Paths



Equivalent behavior with pad or seal ring !!!

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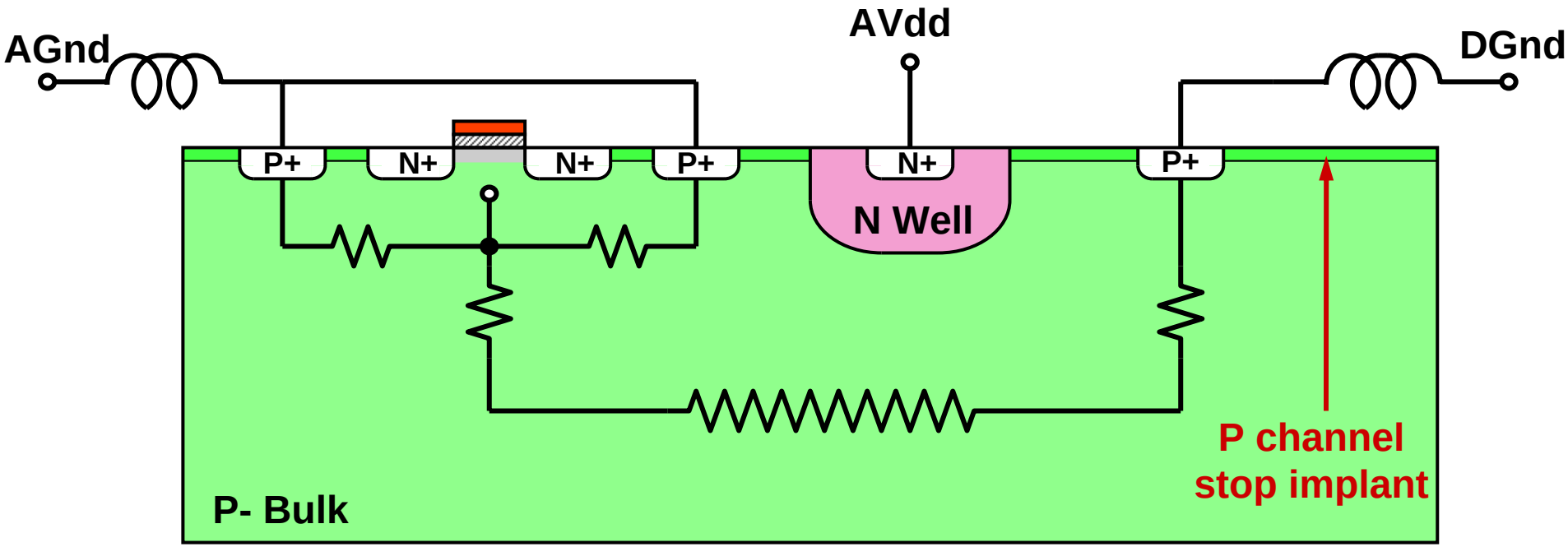
Guard Rings in a Lightly-Doped Process



- Guard rings are more effective in a lightly doped process
- A well region can break the channel stop and increase the isolation

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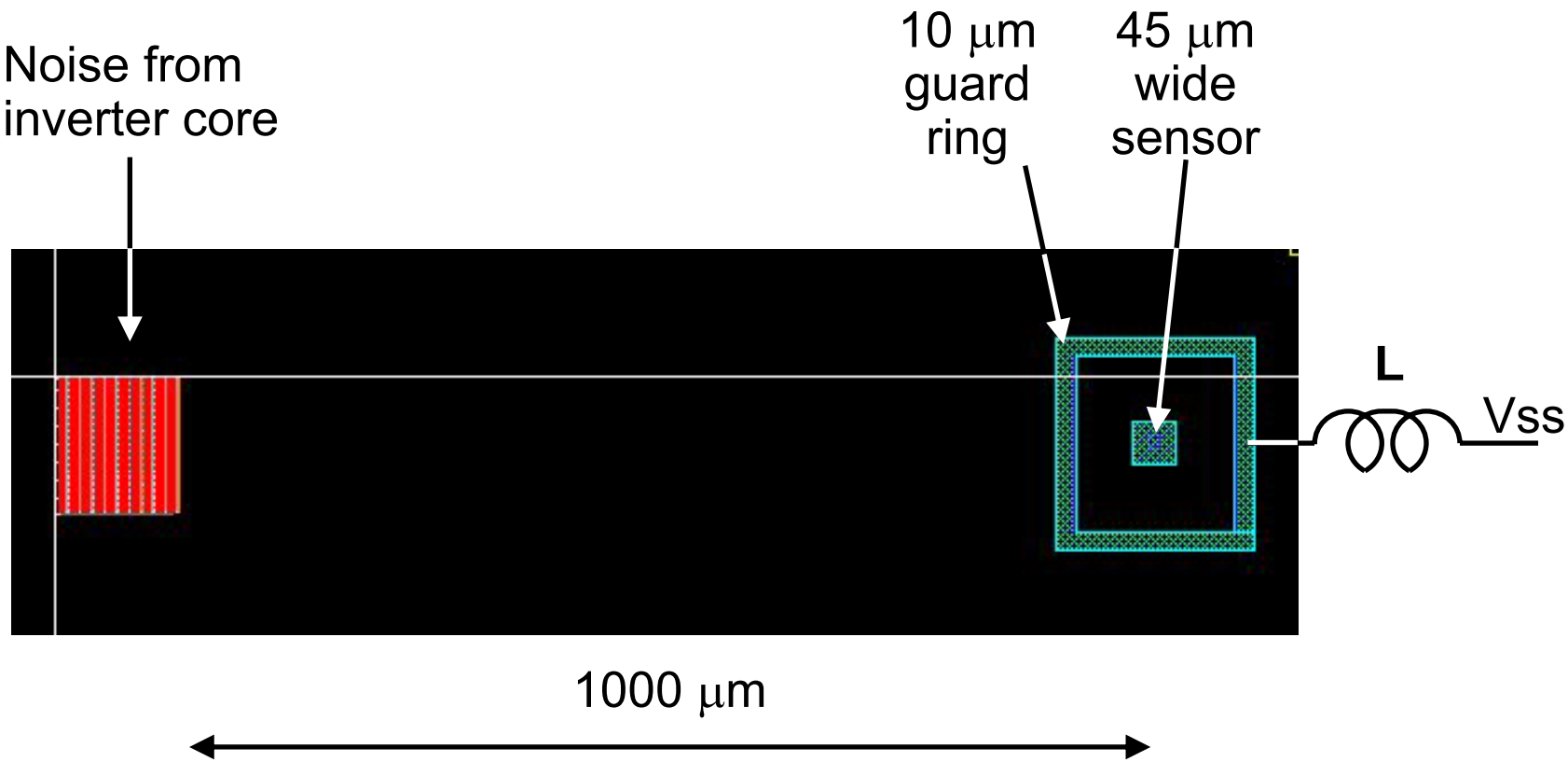
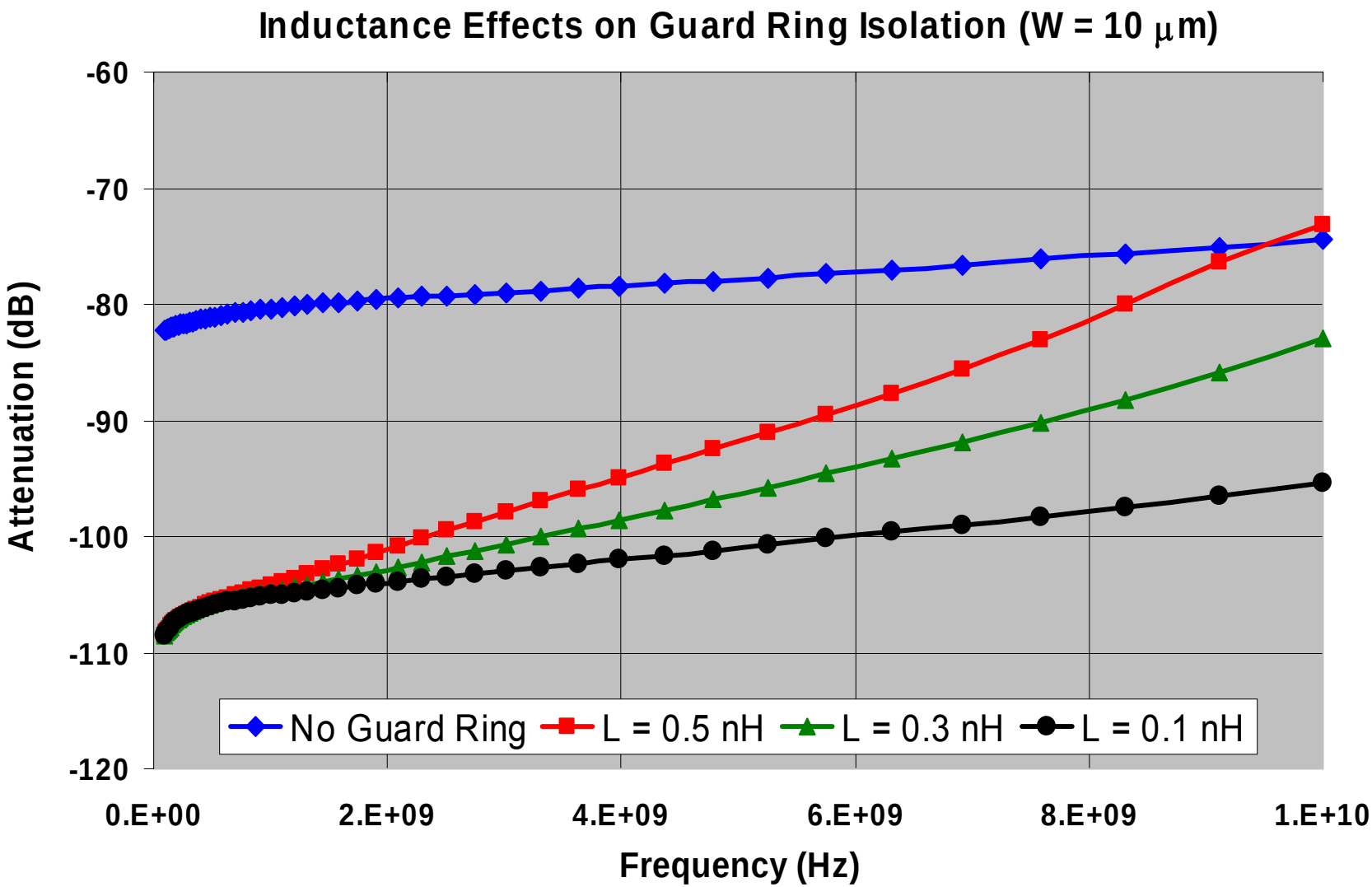
Guard Ring Inductance Simulation Structure



Guard Ring Inductance Simulations



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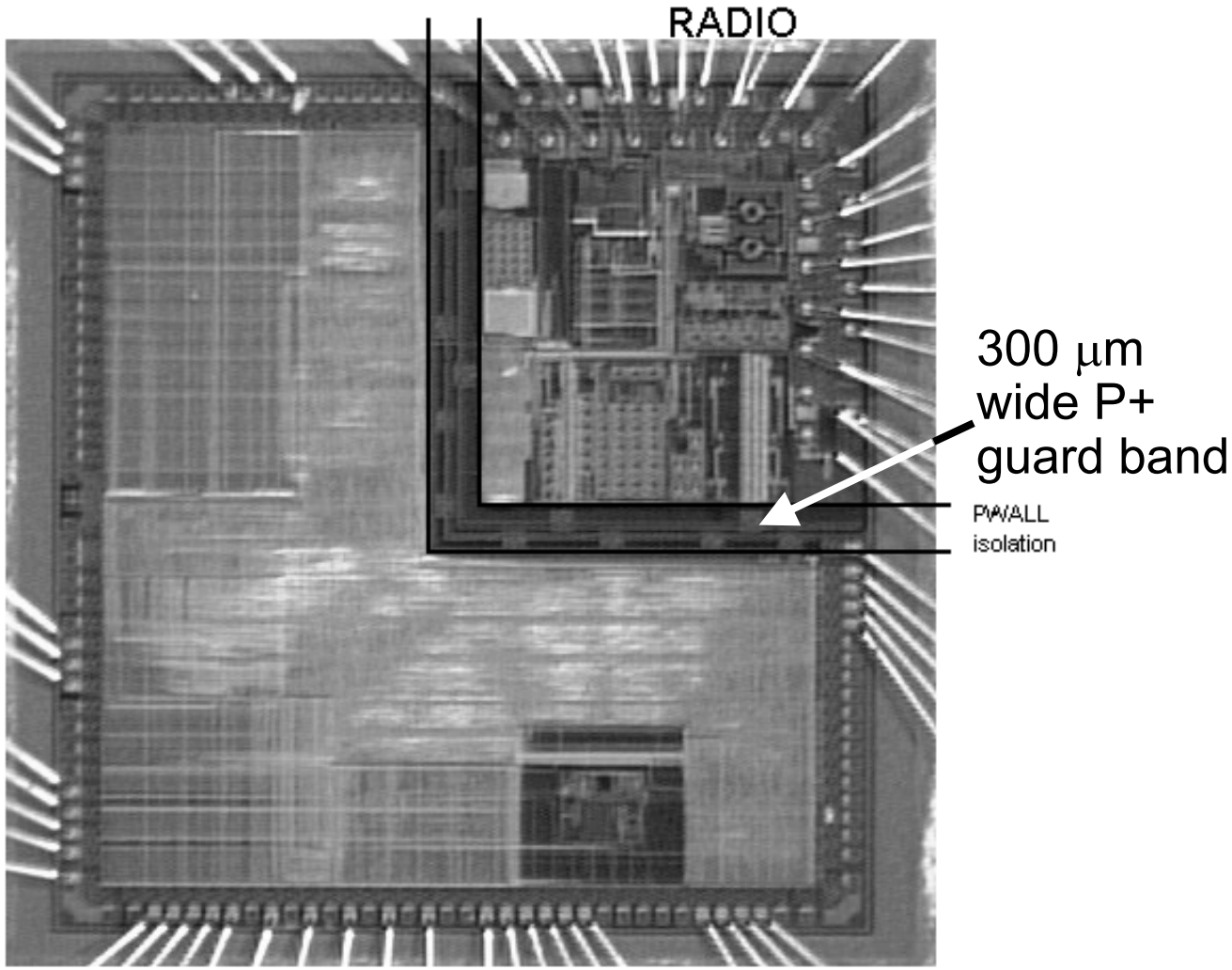
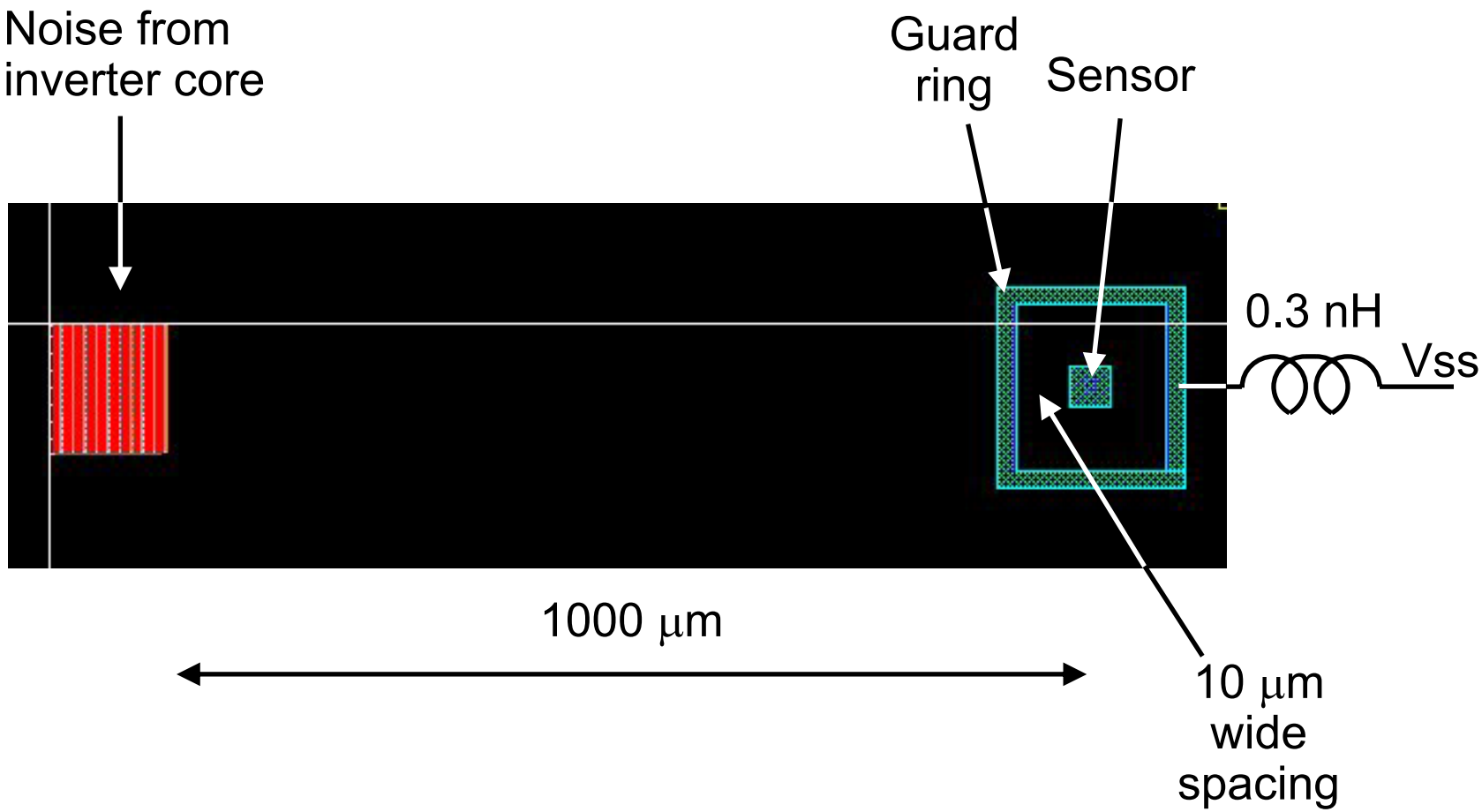
Ericsson & STMicroelectronics: Single-chip BLUETOOTH ASIC

- 0.18 μm CMOS
- 2.5 – 3.0 V
- 75 mW in RX
- 90 mW in TX
- 2 MHz IF
- 5 GHz VCO
- 5.5 mm^2
- Special attention to crosstalk



P. van Zeijl, ISSCC 2002 Tallis Blalack, BCTM 2002, Paper 12.1

Guard Ring Width Simulation Structure



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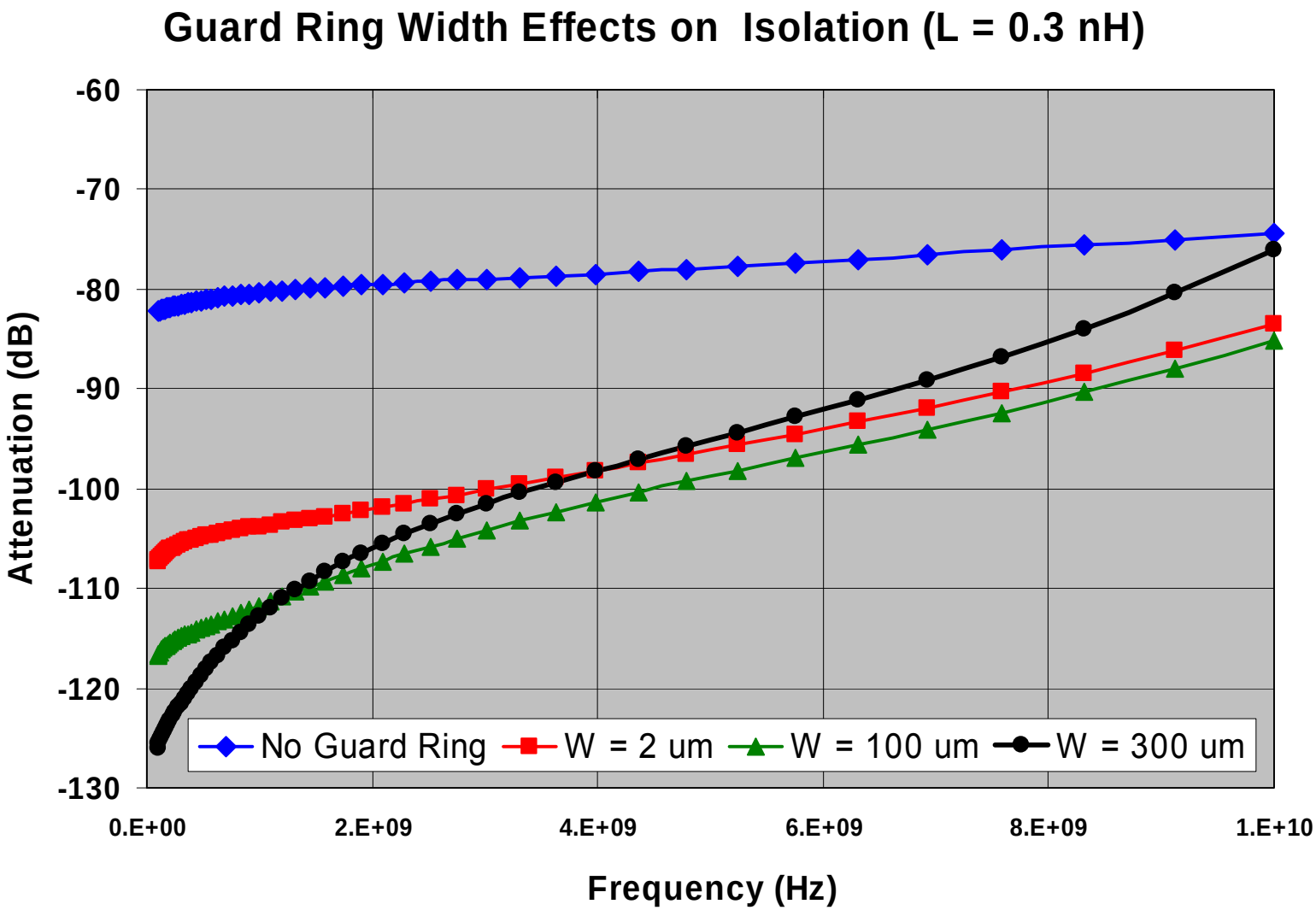
Guard Ring Width Simulations



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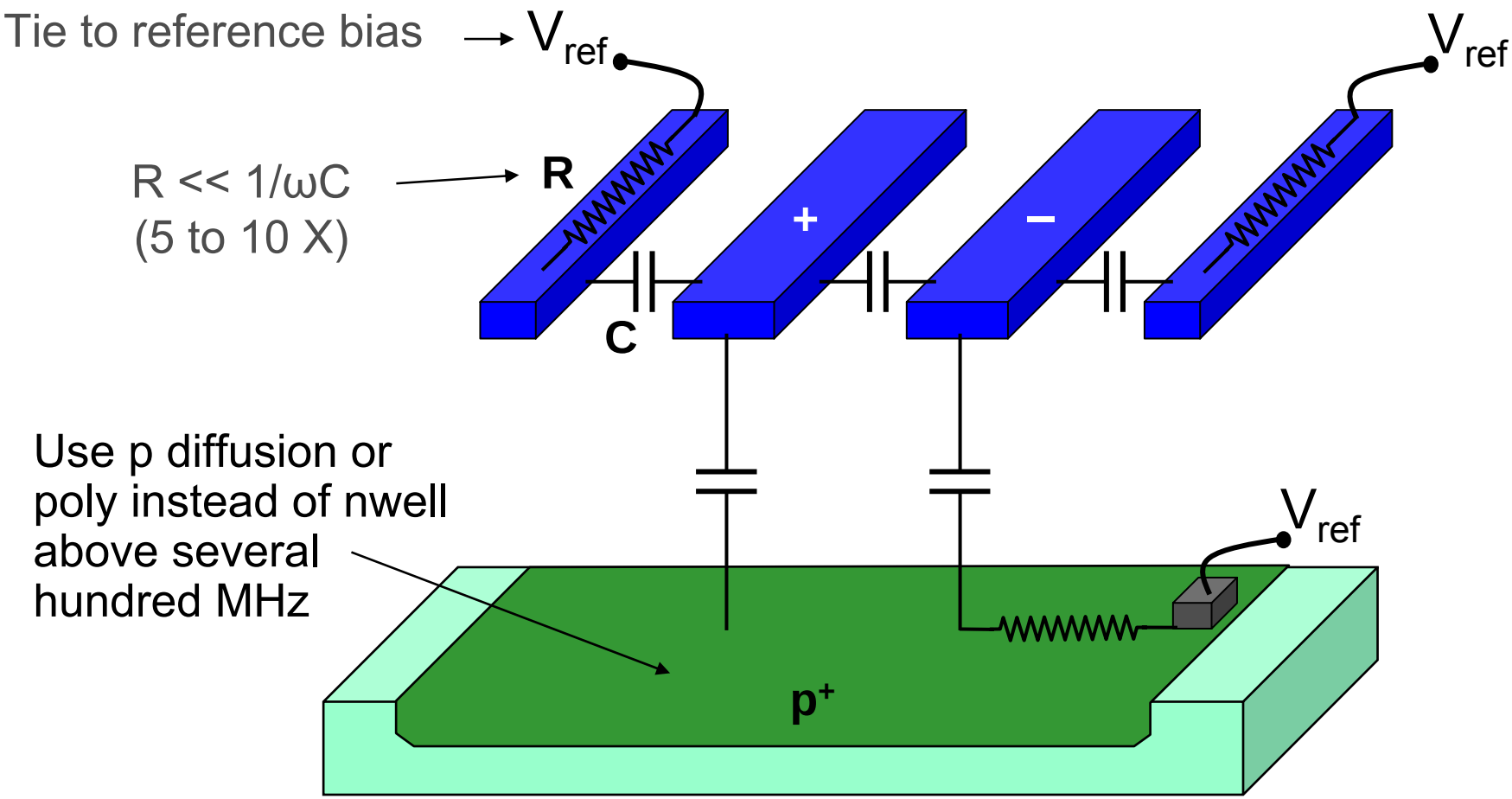
Guard Ring Isolation Summary

The maximum achievable guard ring isolation is ?

Dependent on:

- Technology
- Spacing
- Width
- Grounding scheme
- Package parasitics
- …

Shielding of Signal Lines



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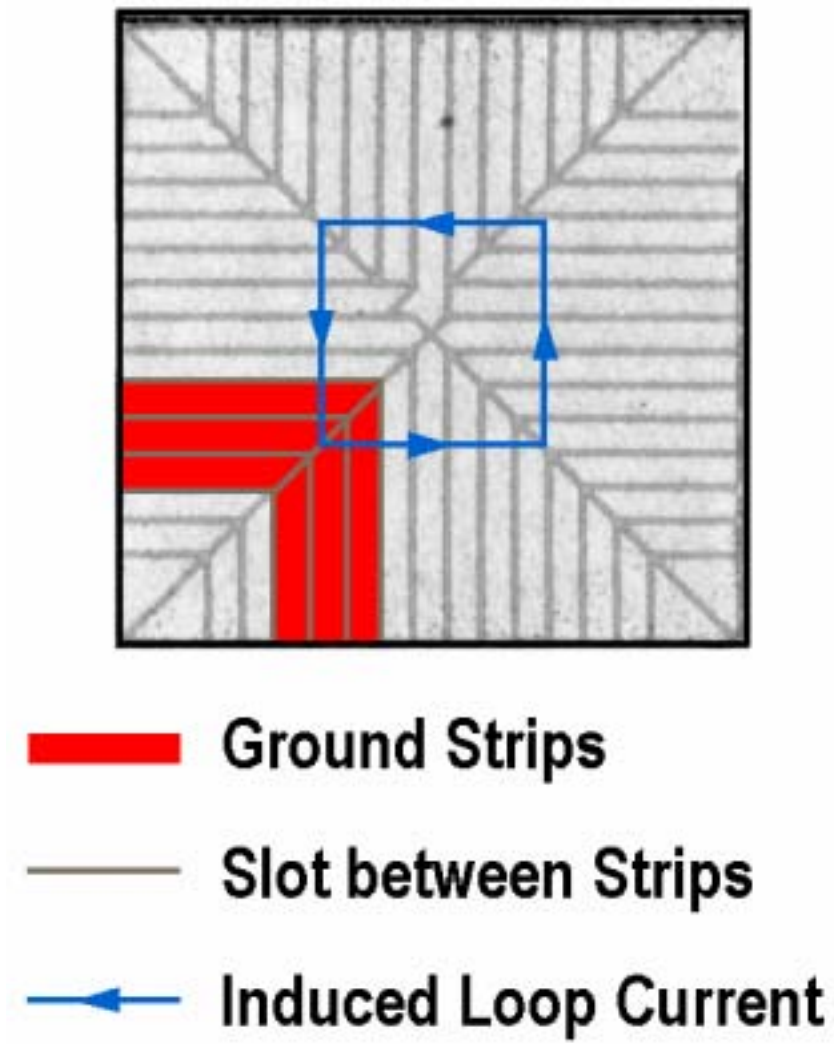
Patterned Ground Shield Design

- Pattern
  - Orthogonal to spiral

    (induced loop current)
- Resistance
  - Low for termination of the electric field
  - Avoid attenuation of the magnetic field



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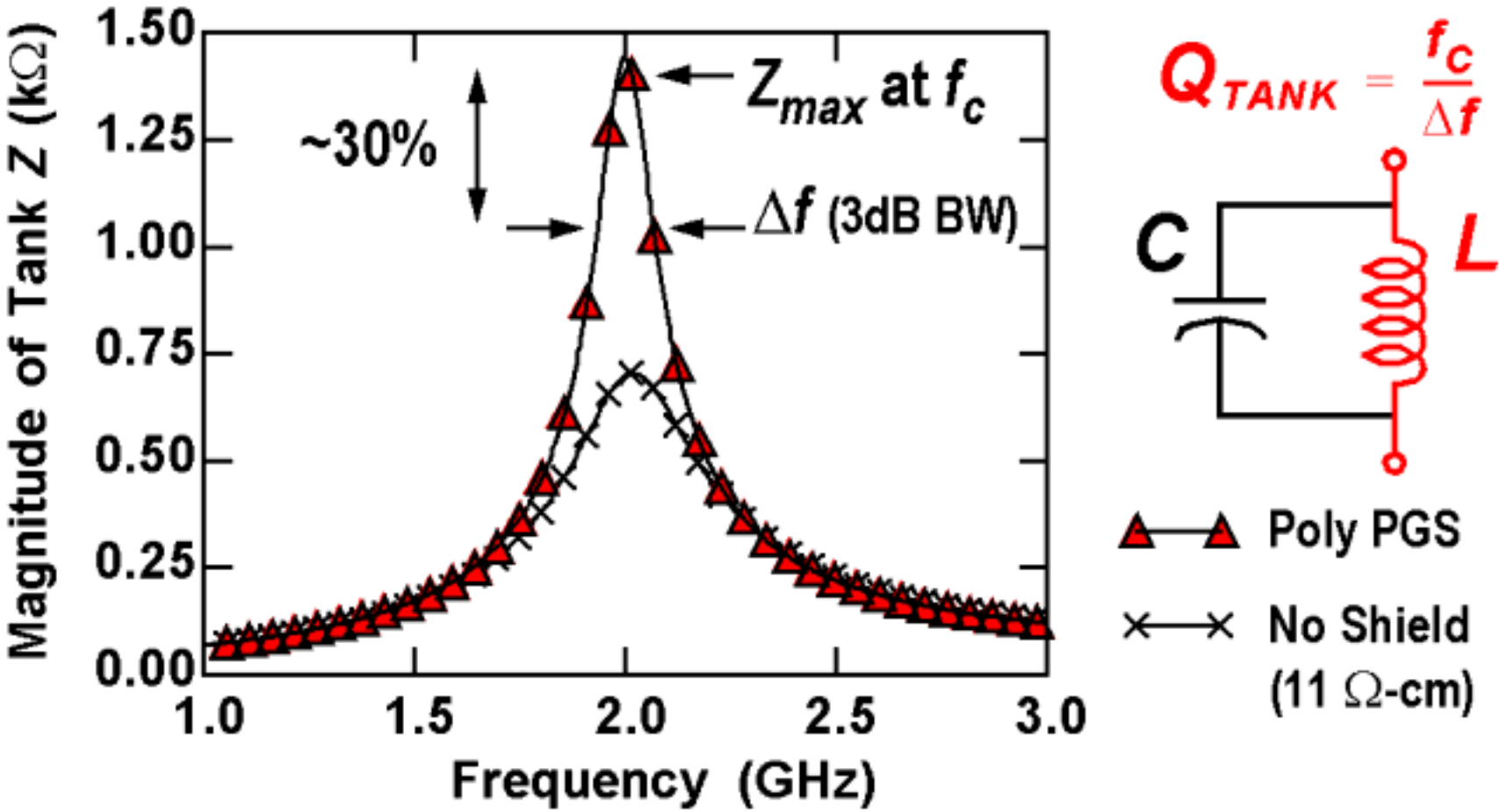
Q Improvement – Tank Impedance Doubled



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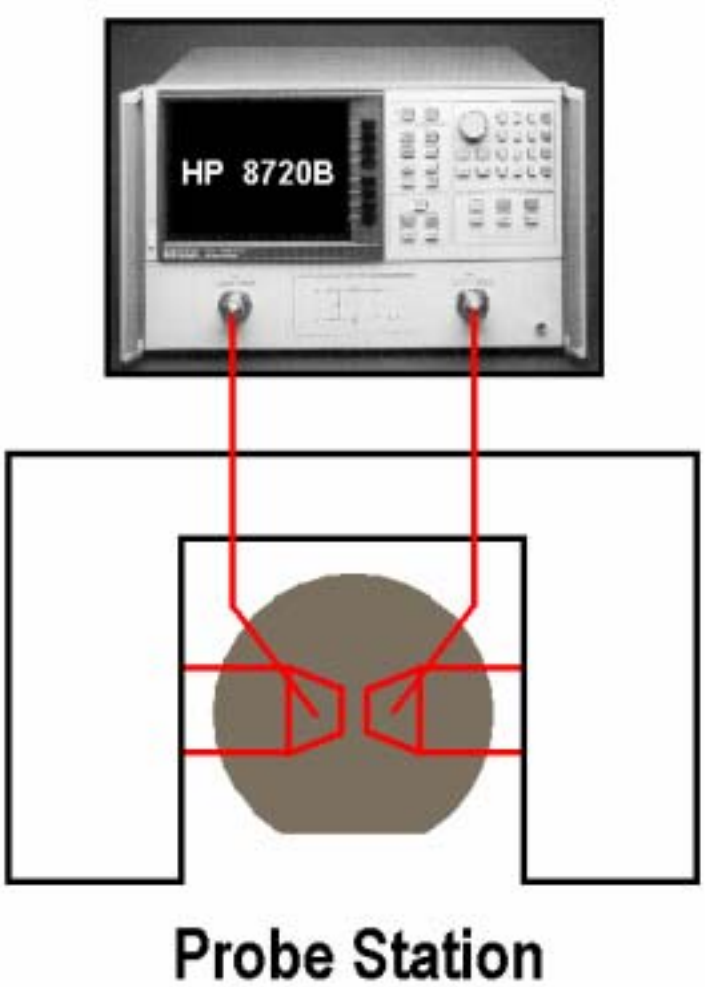
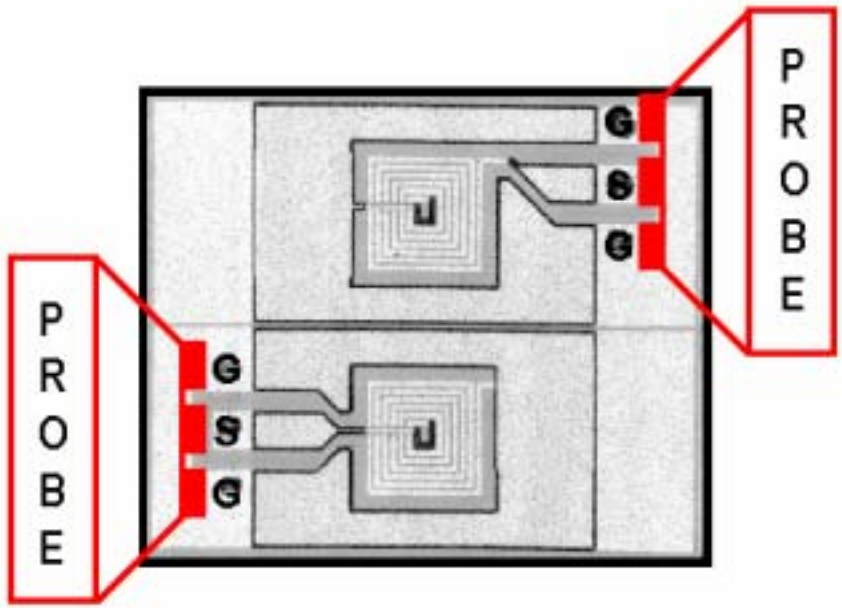
Noise Coupling Measurement





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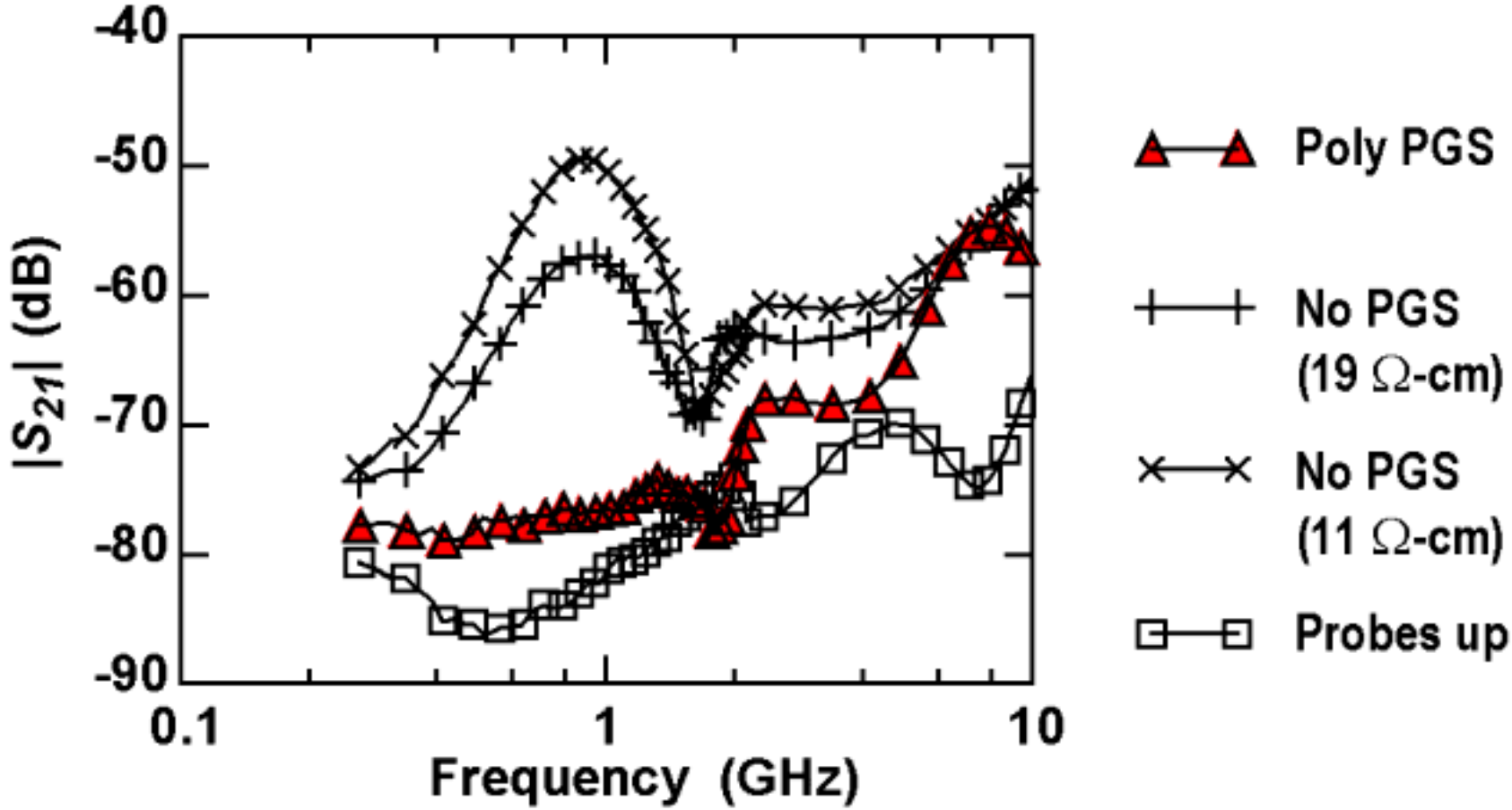
Effect of Polysilicon Ground Shield on Noise Coupling



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Conclusions on Patterned Ground Shield

- Improves Q by eliminating substrate loss
  - up to 33% at 1-2 GHz
- Improves isolation by preventing substrate coupling
  - up to 25 dB at 1 GHz
- Simplifies modeling
- Eliminates substrate dependency
- Requires no additional process steps

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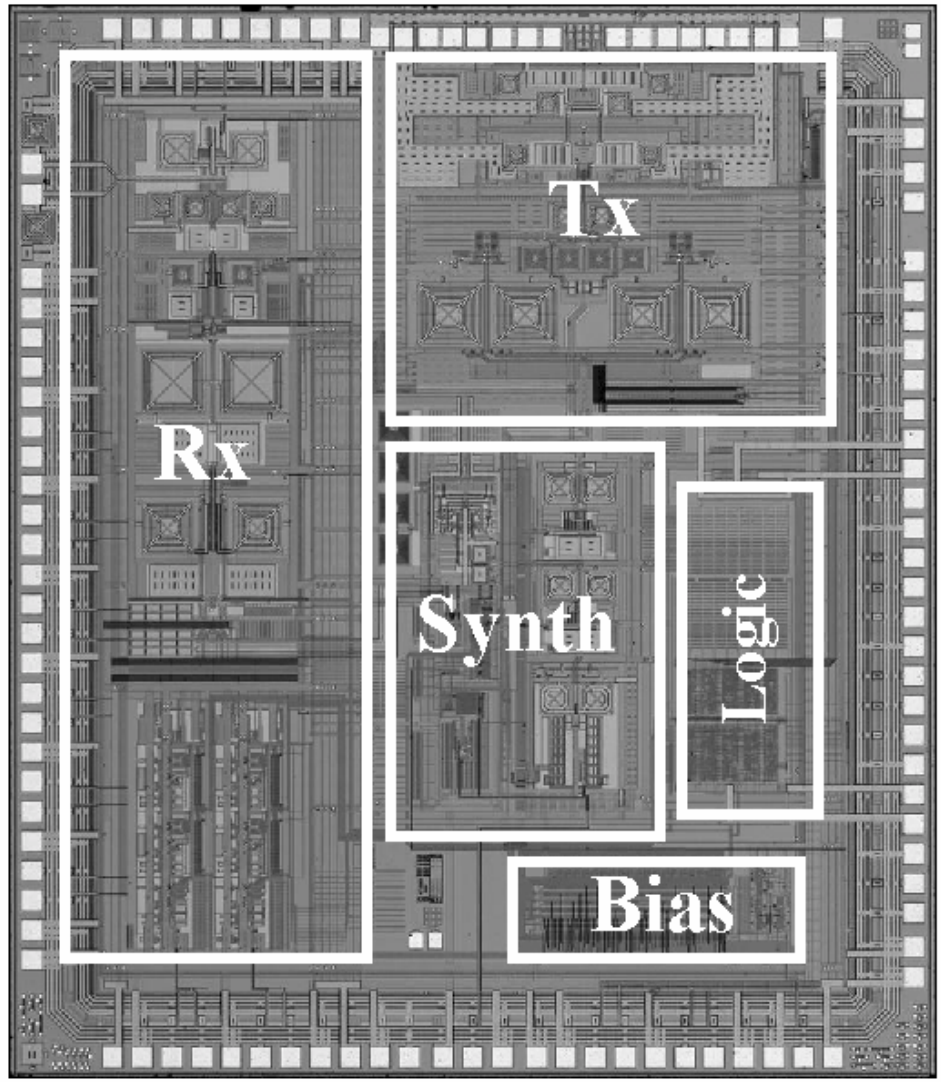
Atheros: 802.11a Radio Transceiver

- 0.25 μm standard digital CMOS for 5 GHz WLAN
- Transmitter 22 dBm output power
- Receiver 8 dB noise figure
- –112dBc/Hz (Δf = 1 MHz)
- 40+ on-chip spirals with PGS
- Shielded RF signals and inductors
- Proper use of guard rings and substrate taps
- Separate supply domains



D. Su, ISSCC 2002

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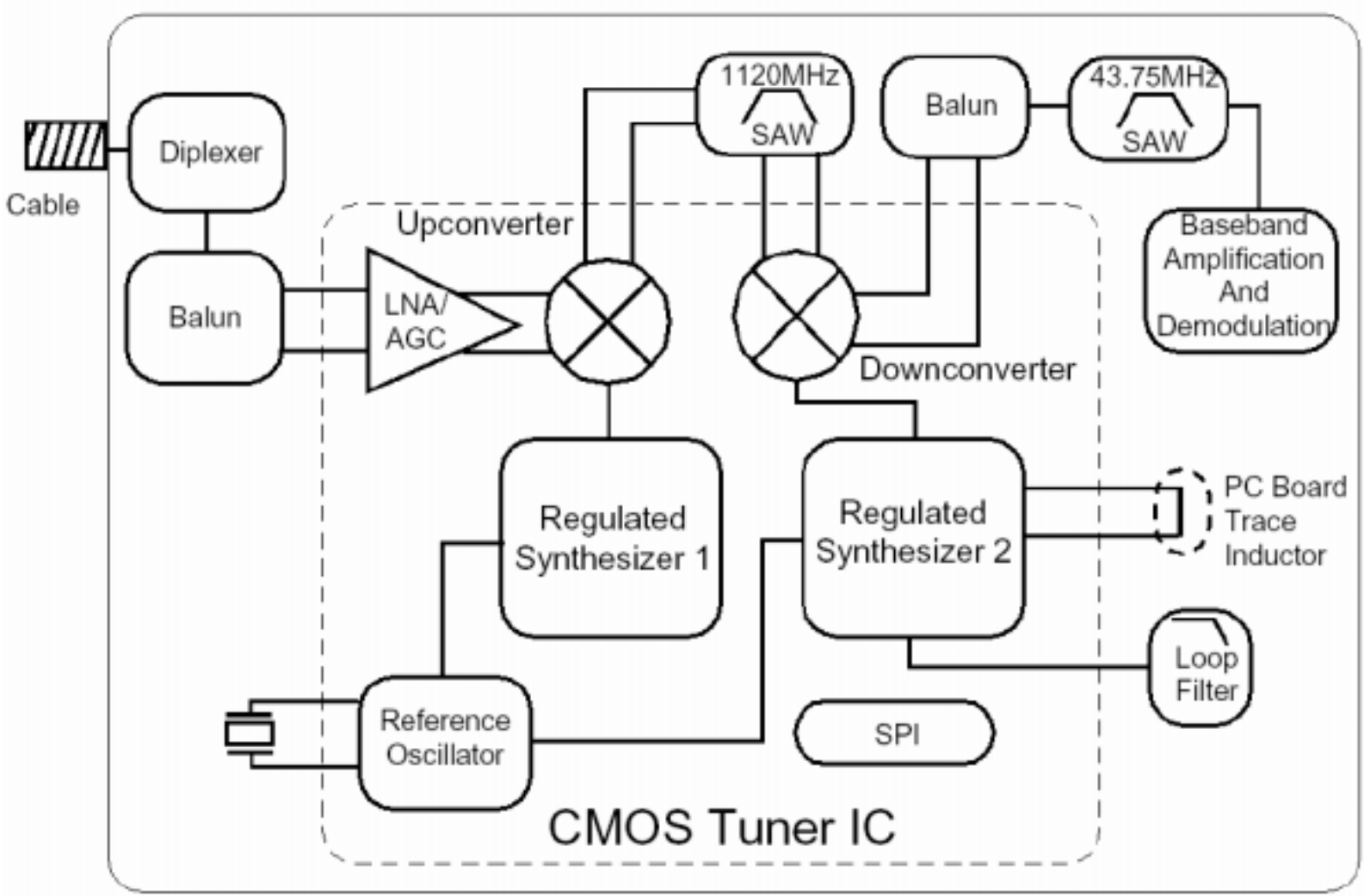
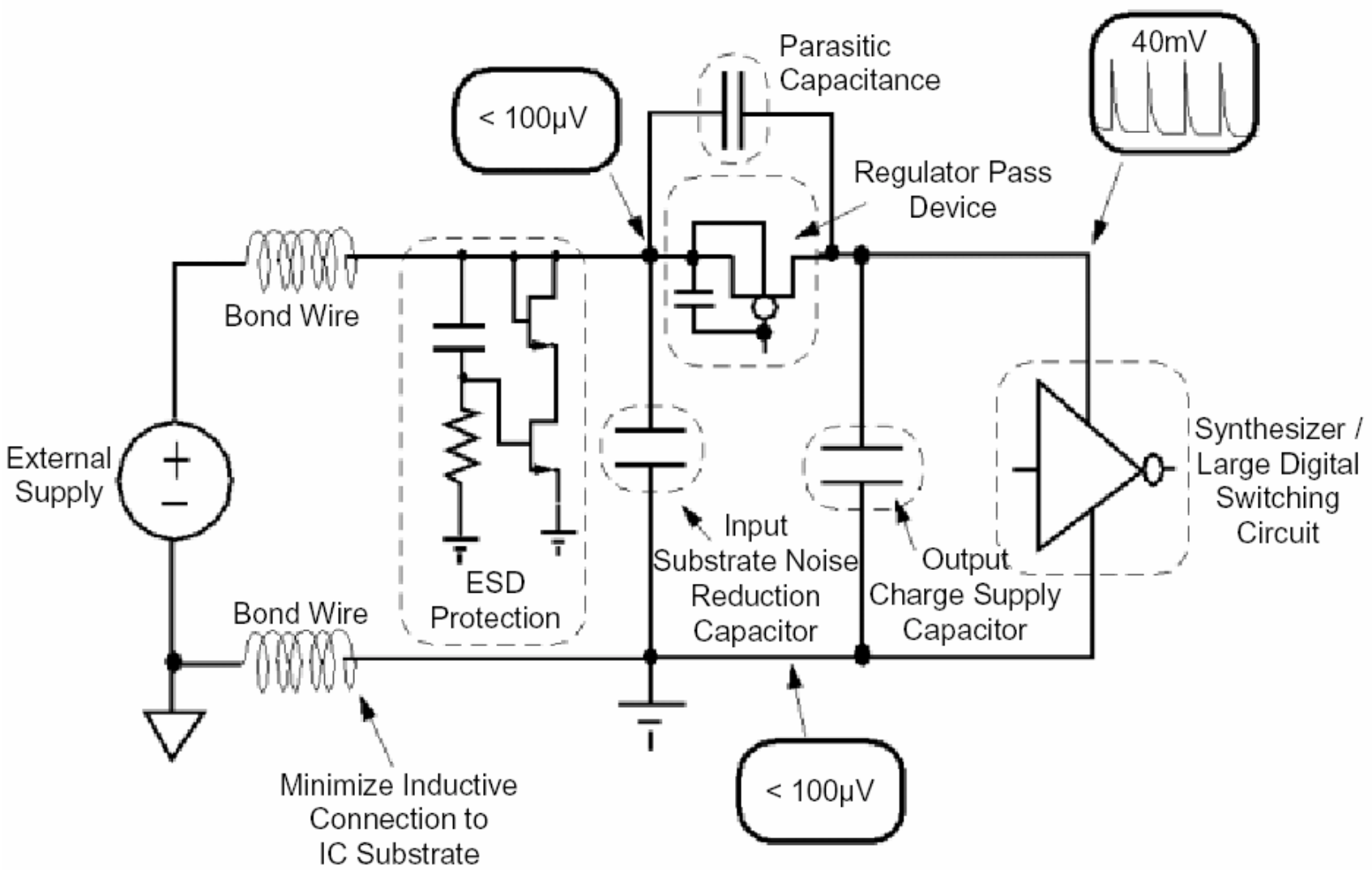
Decoupling Capacitance
Motorola: CMOS Broadband Tuner



L. Connell, ISSCC 2002 Tallis Blalack, BCTM 2002, Paper 12.1

Substrate Noise Suppressing Regulation



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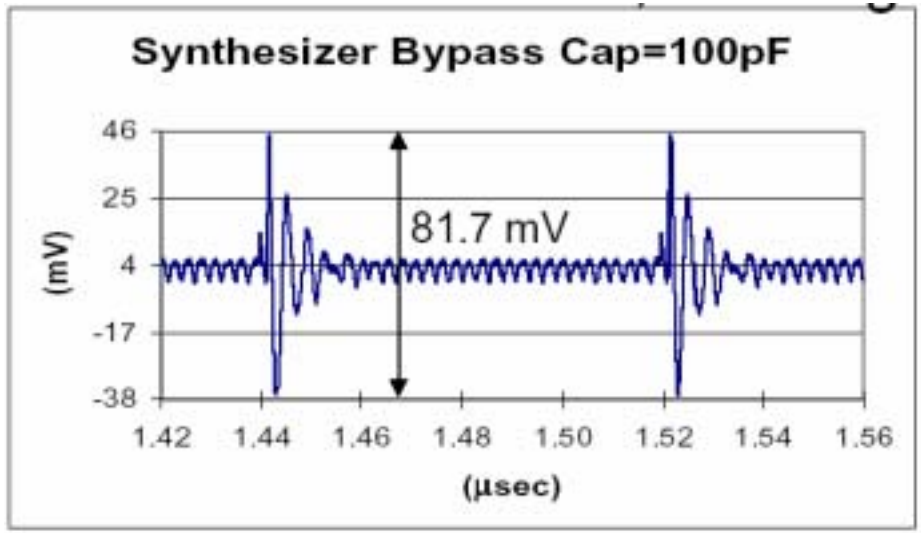
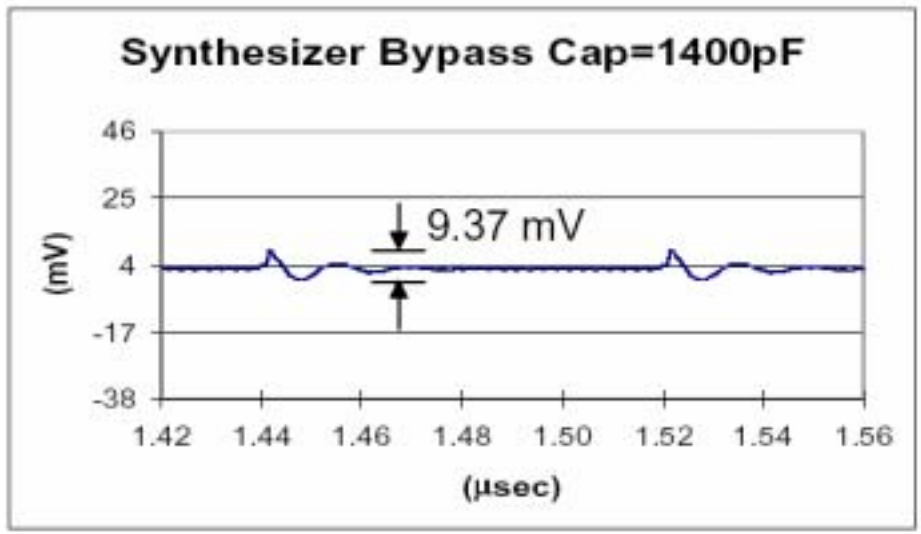
Simulated Substrate Noise, No Regulation

- Low resistivity epi substrate modeled as single node
- Decoupling capacitance used to supply local charge
- Peak current across bond wires much lower
- Ringing on substrate reduced
- ~9x noise reduction
  - ➢ 81.7 mV to 9.37 mV





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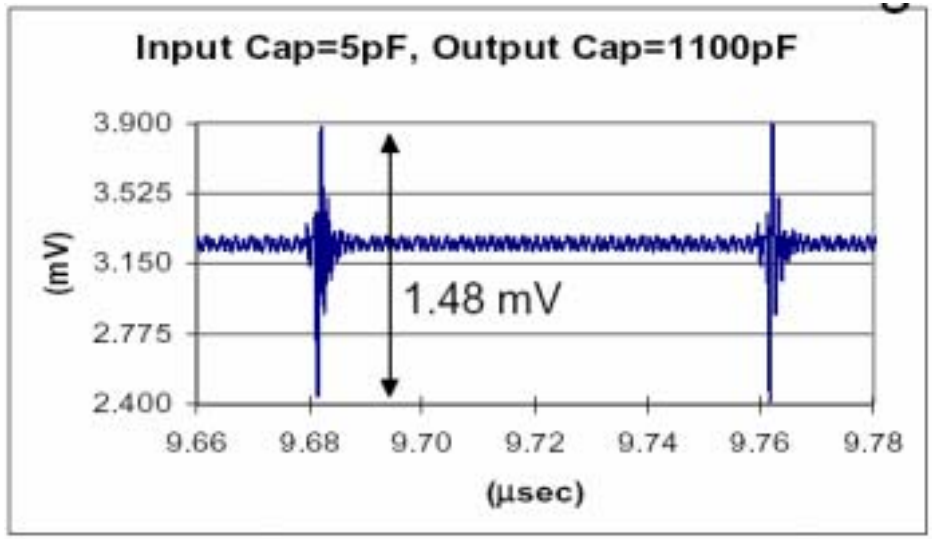
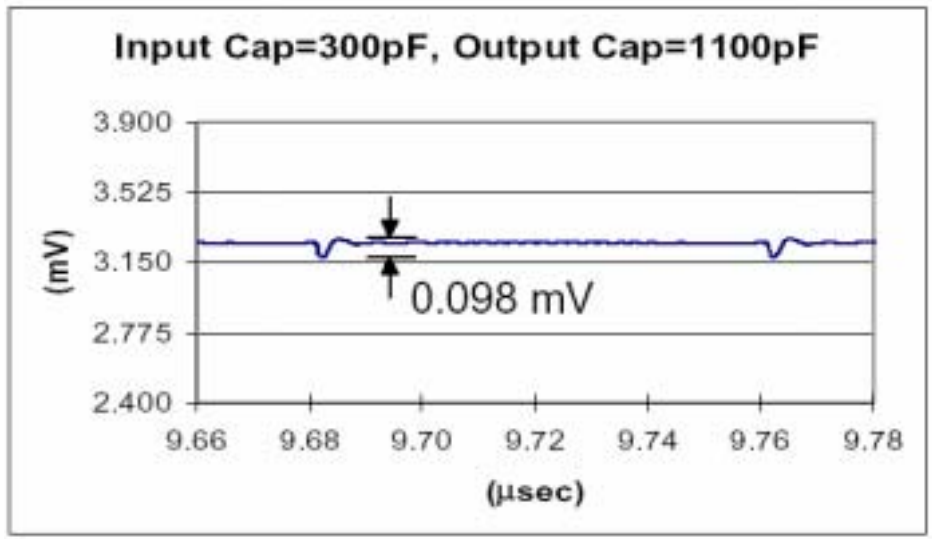
Simulated Substrate Noise with Regulation

- On-chip voltage regulator added
- Decoupling capacitance at input and output of regulator
- ~100x reduction of noise
  - 9.37 mV to 0.098 mV
- Minimized inductive connection to substrate





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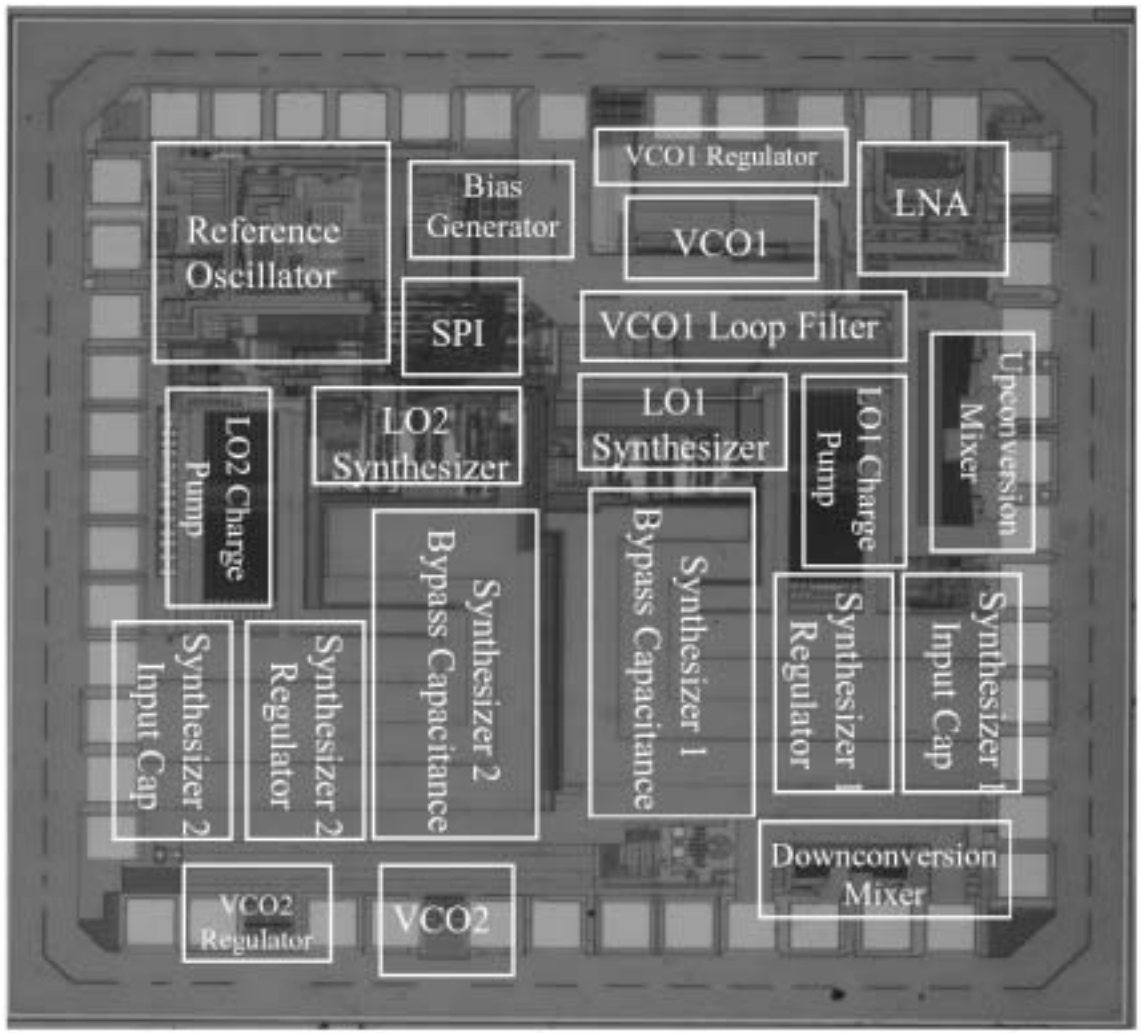
Motorola: CMOS Broadband Tuner

- Synthesizer generates 100 mA switching currents @ 12.5 MHz
- 50 – 860 MHz LNA
- 0.35 μm CMOS
  - heavily doped bulk
- 5 V supply
- 1.5 Watts
- 5 mm^2
- 48 pin eTQFP

~25% of area to reduce substrate noise ~1000x

➢ 81.7 mV to 98 μV



Tallis Blalack, BCTM 2002, Paper 12.1

On-chip RF Isolation Summary

cadence

IT DEPENDS on

- Technology
- Frequency
- Grounding scheme
- Guard rings
- Package
- Decoupling capacitance
- …

Tallis Blalack, BCTM 2002, Paper 12.1

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